GSV2725

3 Input HDMI 2.0/ Type-C/DisplayPort 1.4 to MIPI/LVDS/TTL Mixed Converter with Loop Out and Embedded MCU

July, 2025

Product Specification

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TABLES

Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV2725 is a high-performance, low-power 3 In to 1 Out HDMI 2.0/DisplayPort 1.4 to MIPI CSI-2/DSI/LVDS/TTL mixed converter with Loop Out. Loop Out can be either HDMI 2.0 or DisplayPort 1.4 Transmitter. By integrating enhanced microcontroller based on RISC-V, GSV2725 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver and HDMI Transmitter supports up to 18Gbps (TMDS, 6G/3Lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV2725 can directly map its receiver/transmitter to USB Type-C interface, and Alternate DisplayPort for Type-C can be supported for Type-C to HDMI application. The superior architecture of GSV2725 provides economical smaller footprint solutions using QFN128, targeting applications of TV/Monitor/Sound bar/Stream box and KVM.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV2725 for its DisplayPort and HDMI ports. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Extraction of HDMI Rx and DisplayPort Rx is supported in GSV2725 for audio processing. With audio sample raw data detection feature, LPCM channel filled with consistent zero raw sample data will be automatically detected and muted.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.0, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

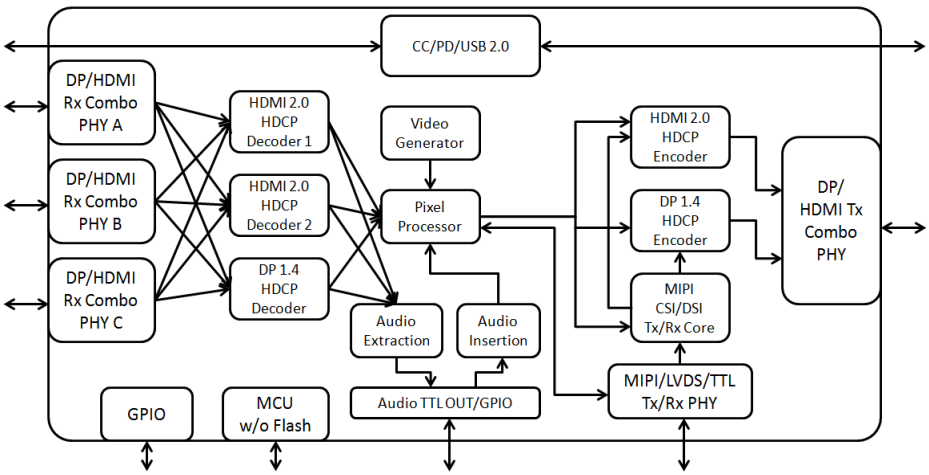


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata

- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.4 HDMI Transmitter Features

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.5 MIPI CSI-2/DSI-2 Transmitter/Receiver

- Support MIPI CSI-2 v3.0 version transmission using D-PHY or C-PHY interface
- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version transmission using D-PHY or C-PHY interface (DSI Tx has no DCS support)

- Support 3.4G bps 1/2/3/4-lane MIPI D-PHY In/Out
- Support Single-Port (1C4D) mode
- Support 5.7G bps 1/2/3-lane MIPI C-PHY Out
- Programmable output swing , slew-rate and pre-emphasis
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.6 Multi-Port LVDS Transmitter/Receiver

- Support Spread Spectrum Clock (SSC)
- Bi-directional LVDS, supports video format up to 4K60 444 10-bit
  - RGB/YCbCr444/YCbCr422/420 can be internally converted to the same color format
- Compatible with series FPGAs' LVDS standard (15 pairs in maximum)
  - Programmable output swing, slew-rate, common voltage and pre-emphasis
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis
  - Data rate up to 1.5Gbps per lane

1.2.7 Compatible TTL Transmitter/Receiver

- 24-bit TTL Video Receiver up to 1080p60 24-bit
  - TTL Schmitt trigger receiver and CMOS receiver selectable
  - SDR/DDR Clock Input available with 0 degree or 90 degree
  - Data rate up to 150Mbps per lane
  - HS/VS/DE available
  - Embedded SAV/EAV mode supported

1.2.8 USB Type-C DisplayPort Alternative Mode Transceiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Dual Role Power Port (DRP)
- Fast Role Swap
- Support Billboard in USB 2.0

1.2.9 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing
- Support 12-10-8 bit Dithering

1.2.10 Audio Output and Input

- I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx /Type-C Rx
- I2S and SPDIF Audio Insertion to HDMI Tx/ DisplayPort Tx /Type-C Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction

1.2.11 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 HDMI 2 Input, Type-C Alt-Mode 1 Input

RxA/RxB are configured as HDMI Rx Input, RxC is configured as Type-C Alt-Mode (DisplayPort) Rx Input. This mode is applicable for monitor application. In this application, All the 2 HDMI RxPort and Type-C Rx can maintain its stream with fast hot-swap without HPD toggling during input switch.

Meanwhile, Audio extraction can be applicable if required.

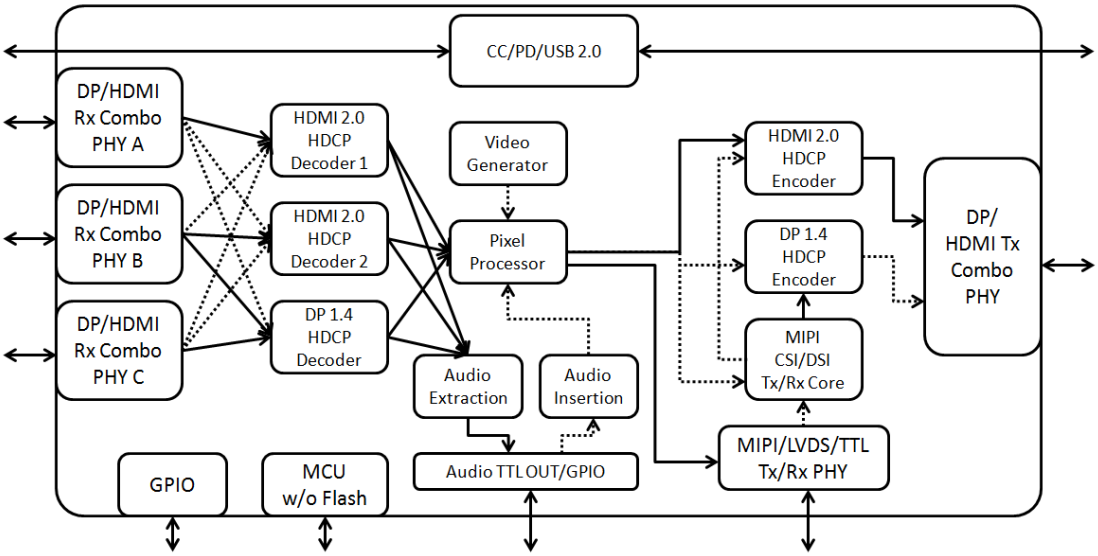


Figure 2. Input Switch Between Different Inputs

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Output	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Output	I2S Data, 5/6 channels
AUD_D3	SDATA[3]	Output	I2S Data, 7/8 channels

AUD_D4	SPDIF	Output	SPDIF channel
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, SPDIF is also capable of sending out with 4 pins.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels
AUD_D1	SPDIF[1]	Output	SPDIF Data[1], 3/4 channels
AUD_D2	SPDIF[2]	Output	SPDIF Data[2], 5/6 channels
AUD_D3	SPDIF[3]	Output	SPDIF Data[3], 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel, 1/2 channels

For TDM format, a fixed format of TDM-8 can be enabled. The Format is listed as below.

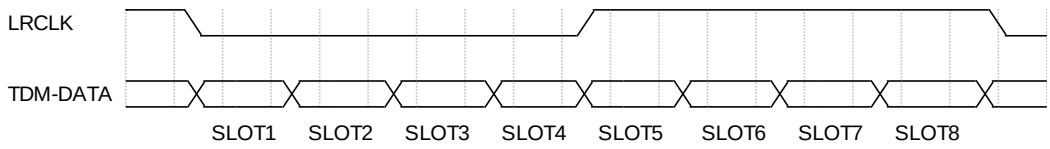


Figure 3. TDM-8 Format

Table 4. TDM Audio Extraction Format

Slot Name	LPCM 2.0 Audio	LPCM 5.1 Audio	LPCM 7.1 Audio
SLOT1	Stereo L	5.1-L	7.1-L
SLOT2	Stereo R	5.1-R	7.1-R
SLOT3		5.1-C	7.1-C
SLOT4		5.1-LFE	7.1-LFE
SLOT5		5.1-LS	7.1-LS
SLOT6		5.1-RS	7.1-RS
SLOT7			7.1-LRS
SLOT8			7.1-RRS

1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted

that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV2725 can detect Sampling Frequency and automatically update it in Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software. General application modes are listed below.

Table 5. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 6. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 7. 8-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Input	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Input	I2S Data, 5/6 channels
AUD_D3	SDATA[3]	Input	I2S Data, 7/8 channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

1.6 Audio Bus Input/Output Bi-Direction Configuration

When bi-direction is needed for a single audio bus, stereo audio insertion and extraction can be simultaneously supported.

Table 8. I2S Audio Insertion and Extraction in Bi-Direction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
AUD_D2	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs
AUD_D3	BCLK	Output	Fixed to 64Fs

AUD_D4	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

2. Pin Description

2.1 Pin Diagram

QFN128 Pin definition is defined as below.

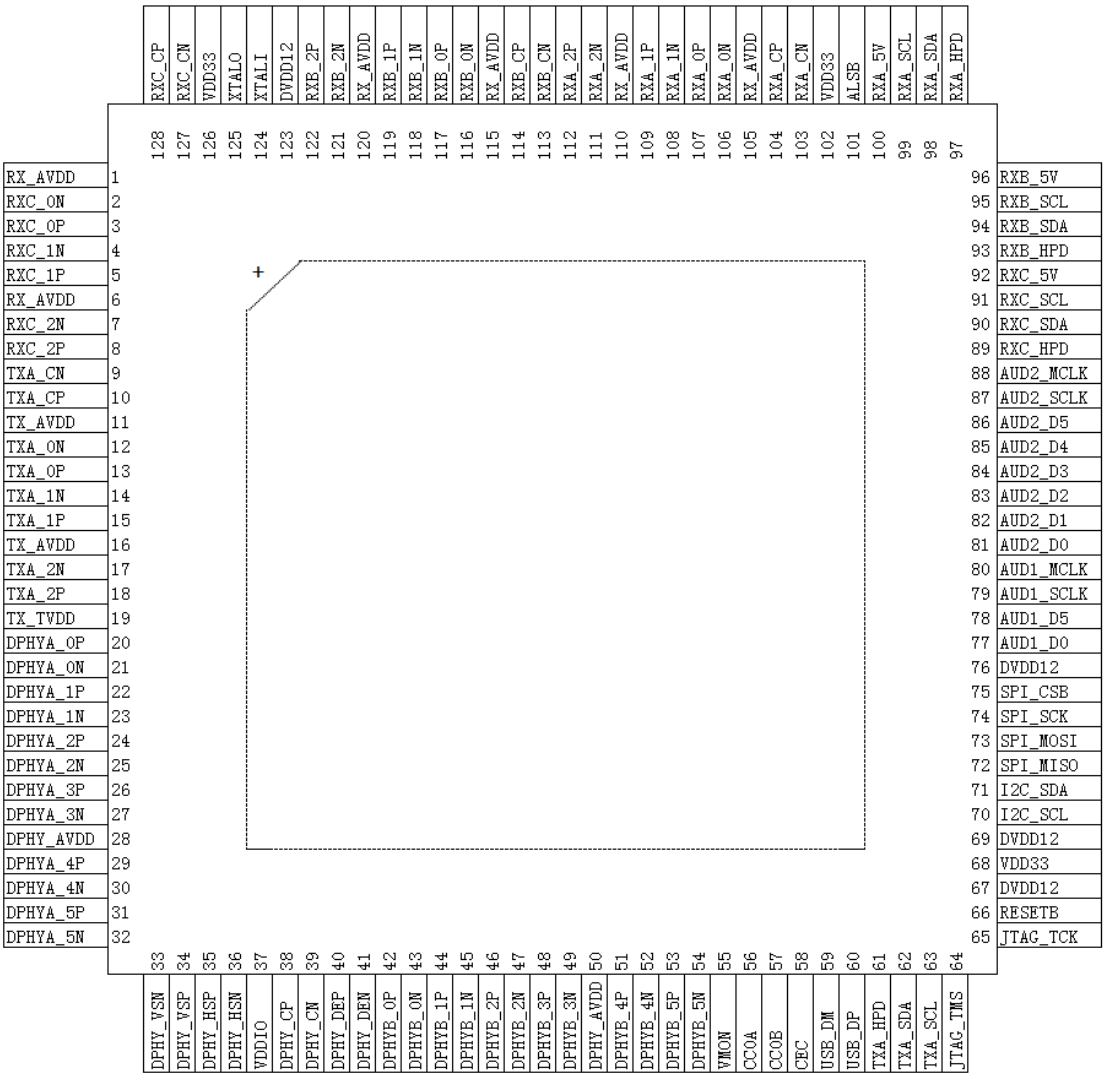


Figure 4. GSV2725 QFN128 Pin Diagram

2.2 QFN128 Pin Description

Table 9. QFN128 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RX Pins/Type-C UFP/DisplayPort RX Pins			
RXA_5V	I	100	HDMI: RXA 5V Detection PAD DP: RXA DP Detection PAD

RXA_HPD	I/O	97	HDMI: RXA HPD PAD DP: RXA HPD PAD
RXA_SDA	I/O	98	HDMI: RXA DDC SDA PAD DP: RXA AUX_P PAD
RXA_SCL	I/O	99	HDMI: RXA DDC SCL PAD DP: RXA AUX_N PAD
RXA_CN	I	103	HDMI: RXA Negative TMDS clock differential input DP: RXA Positive Main-Link differential data input [0]
RXA_CP	I	104	HDMI: RXA Positive TMDS clock differential input DP: RXA Negative Main-Link differential data input [0]
RXA_0N	I	106	HDMI: RXA Negative TMDS differential data input [0] DP: RXA Positive Main-Link differential data input [1]
RXA_0P	I	107	HDMI: RXA Positive TMDS differential data input [0] DP: RXA Negative Main-Link differential data input [1]
RXA_1N	I	108	HDMI: RXA Negative TMDS differential data input [1] DP: RXA Positive Main-Link differential data input [2]
RXA_1P	I	109	HDMI: RXA Positive TMDS differential data input [1] DP: RXA Negative Main-Link differential data input [2]
RXA_2N	I	111	HDMI: RXA Negative TMDS differential data input [2] DP: RXA Positive Main-Link differential data input [3]
RXA_2P	I	112	HDMI: RXA Positive TMDS differential data input [2] DP: RXA Negative Main-Link differential data input [3]
RXB_5V	I	96	HDMI: RXB 5V Detection PAD DP: RXB DP Detection PAD
RXB_HPD	I/O	93	HDMI: RXB HPD PAD DP: RXB HPD PAD
RXB_SDA	I/O	94	HDMI: RXB DDC SDA PAD DP: RXB AUX_P PAD
RXB_SCL	I/O	95	HDMI: RXB DDC SCL PAD DP: RXB AUX_N PAD
RXB_CN	I	113	HDMI: RXB Negative TMDS clock differential input DP: RXB Positive Main-Link differential data input [0]
RXB_CP	I	114	HDMI: RXB Positive TMDS clock differential input DP: RXB Negative Main-Link differential data input [0]
RXB_0N	I	116	HDMI: RXB Negative TMDS differential data input [0] DP: RXB Positive Main-Link differential data input [1]

RXB_0P	I	117	HDMI: RXB Positive TMDS differential data input [0] DP: RXB Negative Main-Link differential data input [1]
RXB_1N	I	118	HDMI: RXB Negative TMDS differential data input [1] DP: RXB Positive Main-Link differential data input [2]
RXB_1P	I	119	HDMI: RXB Positive TMDS differential data input [1] DP: RXB Negative Main-Link differential data input [2]
RXB_2N	I	121	HDMI: RXB Negative TMDS differential data input [2] DP: RXB Positive Main-Link differential data input [3]
RXB_2P	I	122	HDMI: RXB Positive TMDS differential data input [2] DP: RXB Negative Main-Link differential data input [3]
RXC_5V	I	92	HDMI: RXC 5V Detection PAD DP: RXC DP Detection PAD
RXC_HPD	I/O	89	HDMI: RXC HPD PAD DP: RXC HPD PAD
RXC_SDA	I/O	90	HDMI: RXC DDC SDA PAD DP: RXC AUX_P PAD
RXC_SCL	I/O	91	HDMI: RXC DDC SCL PAD DP: RXC AUX_N PAD
RXC_CN	I	127	HDMI: RXC Negative TMDS clock differential input DP: RXC Positive Main-Link differential data input [0]
RXC_CP	I	128	HDMI: RXC Positive TMDS clock differential input DP: RXC Negative Main-Link differential data input [0]
RXC_0N	I	2	HDMI: RXC Negative TMDS differential data input [0] DP: RXC Positive Main-Link differential data input [1]
RXC_0P	I	3	HDMI: RXC Positive TMDS differential data input [0] DP: RXC Negative Main-Link differential data input [1]
RXC_1N	I	4	HDMI: RXC Negative TMDS differential data input [1] DP: RXC Positive Main-Link differential data input [2]
RXC_1P	I	5	HDMI: RXC Positive TMDS differential data input [1] DP: RXC Negative Main-Link differential data input [2]
RXC_2N	I	7	HDMI: RXC Negative TMDS differential data input [2] DP: RXC Positive Main-Link differential data input [3]
RXC_2P	I	8	HDMI: RXC Positive TMDS differential data input [2] DP: RXC Negative Main-Link differential data input [3]
HDMI TX Pins/ Type-C DFP/DisplayPort TX Pins			
TXA_SDA	I/O	62	HDMI: TXA DDC SDA PAD DP: TXA AUX_P PAD

TXA_SCL	O	63	HDMI: TXA DDC SCL PAD DP: TXA AUX_N PAD
TXA_HPD	I	61	HDMI: TXA HPD PAD DP: TXA HPD PAD
CEC	I/O	58	CEC Pad
TXA_CN	O	9	HDMI: TXA Negative TMDS differential data output [3]/ TMDS clock differential output DP: TXA Negative Main-Link differential data output [3]
TXA_CP	O	10	HDMI: TXA Positive TMDS differential data output [3]/ TMDS clock differential output DP: TXA Positive Main-Link differential data output [3]
TXA_0N	O	12	HDMI: TXA Negative TMDS differential data output [0] DP: TXA Negative Main-Link differential data output [2]
TXA_0P	O	13	HDMI: TXA Positive TMDS differential data output [0] DP: TXA Positive Main-Link differential data output [2]
TXA_1N	O	14	HDMI: TXA Negative TMDS differential data output [1] DP: TXA Negative Main-Link differential data output [1]
TXA_1P	O	15	HDMI: TXA Positive TMDS differential data output [1] DP: TXA Positive Main-Link differential data output [1]
TXA_2N	O	17	HDMI: TXA Negative TMDS differential data output [2] DP: TXA Negative Main-Link differential data output [0]
TXA_2P	O	18	HDMI: TXA Positive TMDS differential data output [2] DP: TXA Positive Main-Link differential data output [0]
Power/Ground Pins			
DVDD12	Power	67,69, 76,123	Digital 1.2V voltage power supply
VDDIO	Power	37	Analog 3.3V voltage power supply for Parallel Port
VDD33	Power	68,102, 126	Analog/Digital 3.3V voltage power supply
RX_AVDD	Power	1,6,105, 110,115, 120	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	11,16	Analog 1.2V voltage power supply for TX Port
TX_TVDD	Power	19	Analog 3.3V voltage power supply for TX Port
DPHY_AVDD	Power	28,50,	Analog 1.2V voltage power supply for Parallel Port
MIPI/LVDS/TTL Tx/Rx Pins			

DPHY_CP	I/O	38	LVDS: LVDS clock differential positive output TTL: LVDS clock output
DPHY_CN	I/O	39	LVDS: LVDS clock differential negative output
DPHY_DEN	I/O	41	LVDS: LVDS differential negative LVDS DE
DPHY_DEP	I/O	40	LVDS: LVDS differential positive LVDS DE TTL: Video In/Out, TTL DE
DPHY_VSN	I/O	33	LVDS: LVDS differential negative LVDS VSYNC
DPHY_VSP	I/O	34	LVDS: LVDS differential positive LVDS VSYNC TTL: Video In/Out, TTL VSYNC
DPHY_HSN	I/O	36	LVDS: LVDS differential negative LVDS HSYNC
DPHY_HSP	I/O	35	LVDS: LVDS differential positive LVDS HSYNC TTL: Video In/Out, HSYNC
DPHYA_0P	I/O	20	MIPI: PORTA D-PHY Data[0] differential positive output MIPI: PORTA C-PHY Data[0]-A output LVDS: Video In/Out, Positive LVDS Data[0] VESA: PORTA Positive LVDS Data[0] TTL: Video In/Out, TTL Data[0] Alternate: Digital IO PAD as GPIO0
DPHYA_0N	I/O	21	MIPI: PORTA D-PHY Data[0] differential negative output MIPI: PORTA C-PHY Data[0]-B output LVDS: Video In/Out, Negative LVDS Data[0] VESA: PORTA Negative LVDS Data[0] TTL: Video In/Out, TTL Data[1] Alternate: Digital IO PAD as GPIO1
DPHYA_1P	I/O	22	MIPI: PORTA D-PHY Data[1] differential positive output MIPI: PORTA C-PHY Data[0]-C output LVDS: Video In/Out, Positive LVDS Data[1] VESA: PORTA Positive LVDS Data[1] TTL: Video In/Out, TTL Data[2] Alternate: Digital IO PAD as GPIO2
DPHYA_1N	I/O	23	MIPI: PORTA D-PHY Data[1] differential negative output MIPI: PORTA C-PHY Data[1]-A output LVDS: Video In/Out, Negative LVDS Data[1] VESA: PORTA Negative LVDS Data[1] TTL: Video In/Out, TTL Data[3] Alternate: Digital IO PAD as GPIO3

DPHYA_2P	I/O	24	MIPI: PORTA D-PHY clock differential positive output MIPI: PORTA C-PHY Data[1]-B output LVDS: Video In/Out, Positive LVDS Data[2] VESA: PORTA Positive LVDS Clock TTL: Video In/Out, TTL Data[4] Alternate: Digital IO PAD as GPIO4
DPHYA_2N	I/O	25	MIPI: PORTA D-PHY clock differential negative output MIPI: PORTA C-PHY Data[1]-C output LVDS: Video In/Out, Negative LVDS Data[2] VESA: PORTA Negative LVDS Clock TTL: Video In/Out, TTL Data[5] Alternate: Digital IO PAD as GPIO5
DPHYA_3P	I/O	26	MIPI: PORTA D-PHY Data[2] differential positive output MIPI: PORTA C-PHY Data[2]-A output LVDS: Video In/Out, Positive LVDS Data[3] VESA: PORTA Positive LVDS Data[2] TTL: Video In/Out, TTL Data[6] Alternate: Digital IO PAD as GPIO6
DPHYA_3N	I/O	27	MIPI: PORTA D-PHY Data[2] differential negative output MIPI: PORTA C-PHY Data[2]-B output LVDS: Video In/Out, Negative LVDS Data[3] VESA: PORTA Negative LVDS Data[2] TTL: Video In/Out, TTL Data[7] Alternate: Digital IO PAD as GPIO7
DPHYA_4P	I/O	29	MIPI: PORTA D-PHY Data[3] differential positive output MIPI: PORTA C-PHY Data[2]-C output LVDS: Video In/Out, Positive LVDS Data[4] VESA: PORTA Positive LVDS Data[3] TTL: Video In/Out, TTL Data[8] Alternate: Digital IO PAD as GPIO10
DPHYA_4N	I/O	30	MIPI: PORTA D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[4] VESA: PORTA Negative LVDS Data[3] TTL: Video In/Out, TTL Data[9] Alternate: Digital IO PAD as GPIO11

DPHYA_5P	I/O	31	LVDS: Video In/Out, Positive LVDS Data[5] VESA: PORTA Positive LVDS Data[4] TTL: Video In/Out, TTL Data[10] Alternate: Digital IO PAD as GPIO12
DPHYA_5N	I/O	32	LVDS: Video In/Out, Negative LVDS Data[5] VESA: PORTA Negative LVDS Data[4] TTL: Video In/Out, TTL Data[11] Alternate: Digital IO PAD as GPIO13
DPHYB_0P	I/O	42	MIPI: PORTB D-PHY Data[0] differential positive output MIPI: PORTB C-PHY Data[0]-A output LVDS: Video In/Out, Positive LVDS Data[6] VESA: PORTB Positive LVDS Data[0] TTL: Video In/Out, TTL Data[12] Alternate: Digital IO PAD as GPIO0
DPHYB_0N	I/O	43	MIPI: PORTB D-PHY Data[0] differential negative output MIPI: PORTB C-PHY Data[0]-B output LVDS: Video In/Out, Negative LVDS Data[6] VESA: PORTB Negative LVDS Data[0] TTL: Video In/Out, TTL Data[13] Alternate: Digital IO PAD as GPIO1
DPHYB_1P	I/O	44	MIPI: PORTB D-PHY Data[1] differential positive output MIPI: PORTB C-PHY Data[0]-C output LVDS: Video In/Out, Positive LVDS Data[7] VESA: PORTB Positive LVDS Data[1] TTL: Video In/Out, TTL Data[14] Alternate: Digital IO PAD as GPIO2
DPHYB_1N	I/O	45	MIPI: PORTB D-PHY Data[1] differential negative output MIPI: PORTB C-PHY Data[1]-A output LVDS: Video In/Out, Negative LVDS Data[7] VESA: PORTB Negative LVDS Data[1] TTL: Video In/Out, TTL Data[15] Alternate: Digital IO PAD as GPIO3

DPHYB_2P	I/O	46	MIPI: PORTB D-PHY clock differential positive output MIPI: PORTB C-PHY Data[1]-B output LVDS: Video In/Out, Positive LVDS Data[8] VESA: PORTB Positive LVDS Clock TTL: Video In/Out, TTL Data[16] Alternate: Digital IO PAD as GPIO4
DPHYB_2N	I/O	47	MIPI: PORTB D-PHY clock differential negative output MIPI: PORTB C-PHY Data[1]-C output LVDS: Video In/Out, Negative LVDS Data[8] VESA: PORTB Negative LVDS Clock TTL: Video In/Out, TTL Data[17] Alternate: Digital IO PAD as GPIO5
DPHYB_3P	I/O	48	MIPI: PORTB D-PHY Data[2] differential positive output MIPI: PORTB C-PHY Data[2]-A output LVDS: Video In/Out, Positive LVDS Data[9] VESA: PORTB Positive LVDS Data[2] TTL: Video In/Out, TTL Data[18] Alternate: Digital IO PAD as GPIO6
DPHYB_3N	I/O	49	MIPI: PORTB D-PHY Data[2] differential negative output MIPI: PORTB C-PHY Data[2]-B output LVDS: Video In/Out, Negative LVDS Data[9] VESA: PORTB Negative LVDS Data[2] TTL: Video In/Out, TTL Data[19] Alternate: Digital IO PAD as GPIO7
DPHYB_4P	I/O	51	MIPI: PORTB D-PHY Data[3] differential positive output MIPI: PORTB C-PHY Data[2]-C output LVDS: Video In/Out, Positive LVDS Data[10] VESA: PORTB Positive LVDS Data[3] TTL: Video In/Out, TTL Data[20] Alternate: Digital IO PAD as GPIO10
DPHYB_4N	I/O	52	MIPI: PORTB D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[10] VESA: PORTB Negative LVDS Data[3] TTL: Video In/Out, TTL Data[21] Alternate: Digital IO PAD as GPIO11

DPHYB_5P	I/O	53	LVDS: Video In/Out, Positive LVDS Data[11] VESA: PORTB Positive LVDS Data[4] TTL: Video In/Out, TTL Data[22] Alternate: Digital IO PAD as GPIO12
DPHYB_5N	I/O	54	LVDS: Video In/Out, Negative LVDS Data[11] VESA: PORTB Negative LVDS Data[4] TTL: Video In/Out, TTL Data[23] Alternate: Digital IO PAD as GPIO13
Digital pins			
I2C_SDA	I/O	71	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU
I2C_SCL	I/O	70	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU
AUD1_SCLK	I/O	79	Digital IO PAD Default: SCLK of Audio Bus 1 Alternate 1: GPIO3 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control Alternate 3: DisplayPort Rx 3D Left/Right Indication Pin
AUD1_MCLK	I/O	80	Digital IO PAD Default: MCLK of Audio Bus 1 Alternate 1: GPIO2 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
AUD1_D0	I/O	77	Digital IO PAD Default: Data0 of Audio Bus 1 Alternate 1: GPIO0 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD1_D5	I/O	78	Digital IO PAD Default: Data5 of Audio Bus 1 Alternate 1: GPIO1 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD2_SCLK	I/O	87	Digital IO PAD Default: SCLK of Audio Bus 2 Alternate 1: GPIO5 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control

AUD2_MCLK	I/O	88	Digital IO PAD Default: MCLK of Audio Bus 2 Alternate 1: GPIO4 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
AUD2_D0	I/O	81	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: GPIO7 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD2_D1	I/O	82	Digital IO PAD Default: Data1of Audio Bus 2 Alternate 1: GPIO10 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD2_D2	I/O	83	Digital IO PAD Default: Data2 of Audio Bus 2 Alternate 1: GPIO11 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD2_D3	I/O	84	Digital IO PAD Default: Data3 of Audio Bus 2 Alternate 1: GPIO12 for internal MCU control Alternate 2: Advanced Timer1 for internal MCU control
AUD2_D4	I/O	85	Digital IO PAD Default: Data4 of Audio Bus 2 Alternate 1: GPIO13 for internal MCU control Alternate 2: Advanced Timer2 for internal MCU control
AUD2_D5	I/O	86	Digital IO PAD Default: Data5 of Audio Bus 2 Alternate 1: GPIO6 for internal MCU control Alternate 2: UART_RX for internal MCU control Alternate 3: CEC
SPI_CSB	I/O	75	Default: CSB for SPI of external Flash
SPI_SCK	I/O	74	Default: SCK for SPI of external Flash
SPI_MOSI	I/O	73	Digital IO PAD Default: MOSI for SPI of external Flash
SPI_MISO	I/O	72	Digital IO PAD Default: MISO for SPI of external Flash
RESETB	I	66	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	124	25M Crystal Input

XTALO	I/O	125	25M Crystal output
JTAG_TMS	I/O	64	Default: TMS, Internal MCU programming pin Alternate: General Interrupt Output Pin
JTAG_TCK	I	65	Default: TCK, Internal MCU programming pin Alternate: AVMUTE Interrupt Output Pin
VMON	I/O	55	VBus0 Monitor Pin
CC0A	I/O	56	Type-C CC0 Pin1
CC0B	I/O	57	Type-C CC0 Pin2
USB_DP	I/O	60	USB 2.0 D+ Pin
USB_DM	I/O	59	USB 2.0 D- Pin
ALSB	I	101	Voltage signal input, determines 2 LSB of I2C slave address GND: 0 VDD33/3: 1

2.3 Video Pin Mapping

GSV2725 TTL/LVDS can support multiple modes. The mode register is defined as below. These 3 bytes are the key configuration for different pin mapping types.

Table 10. Pin Mapping Mode Register Definition

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Mode CFG 2	N/A	N/A	i2c_tx_par_multi_pixel_sel[1:0]: 00: 1 pixel per clk 01: 2 pixels per clk 10: Reserved 11: Reserved		N/A	i2c_tx_par_clk_ratio[2:0]: Ratio of SDR VCLK/Pixel DIV CLK 000/001: 1 clk 1 pixel = 1x 010: 2 clk 1 pixel = 2x 011: 3 clk 1 pixel = 3x … 111: 7 clk 1 pixel = 7x		
Mode CFG 1	i2c_tx_par_panel_en: 0: Disable 1: Enable	i2c_tx_par_panel_sel: 0: VESA 1: JEIDA	i2c_tx_par_sub_mode[1:0]: 00: Mode A 01: Mode B 10: Mode C 11: Mode D		N/A	i2c_tx_par_422_en: 0: RGB 4:4:4 /CrYCb 4:4:4 /CrYCb 4:2:0 1: 4:2:2	i2c_tx_par_bit_width[1:0]: 00: 6 bits 01: 8 bits 10:10 bits 11:12 bits	
Mode CFG 0	i2c_tx_par_ttl_lvds_sel: 0: TTL 1: LVDS	N/A		i2c_tx_par_sync_mode: 001: ITU Embedded Syncs 000: Separate Syncs	N/A	N/A	i2c_tx_par_vclk_divn_en: 0: div 1 1: div N	i2c_tx_par_vclk_ddr_en: 0: SDR 1: DDR

2.3.1 TTL Output Mode

In TTL mode, Separate Sync and Embedded Sync BT656 and BT1120 timing can be supported in single pixel mode. The maximum pixel frequency is 150MHz, typically 1080p@60Hz.

GSV2725 TTL mode supports video output format modes are listed below.

- All modes support both SDR and DDR
- YCbCr 4:2:2 mode using embedded syncs (BT.1120, BT.656, BTA-T1004) can be supported
- Internal CSC converts all color spaces to unified YCbCr 4:2:2

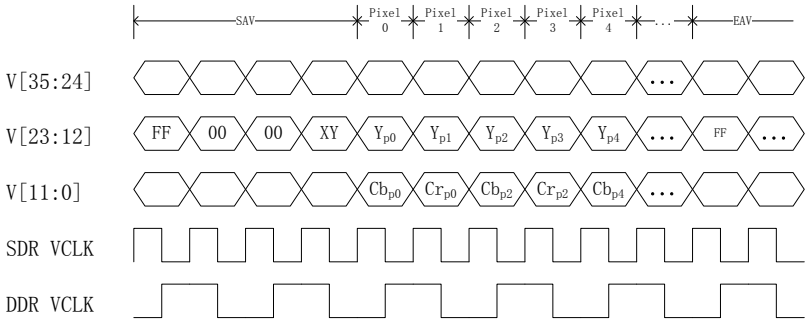


Figure 5. 24-bits YCbCr 4:2:2 BT.1120 Embedded Sync Timing Diagram

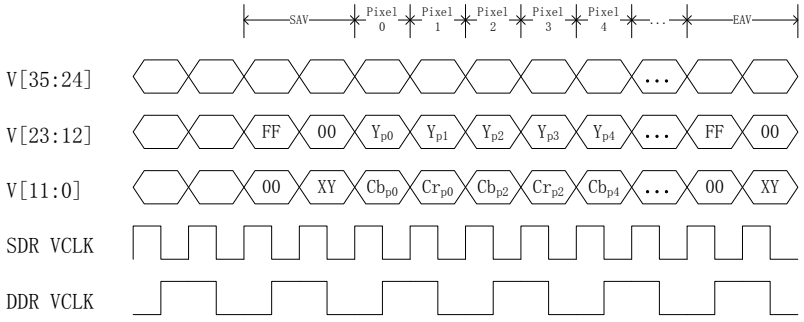


Figure 6. 24-bits YCbCr 4:2:2 BTA-T1004 Embedded Sync Timing Diagram

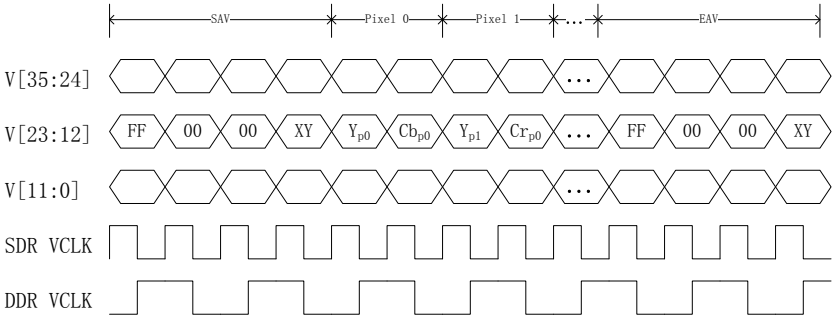


Figure 7. 12-bits YCbCr 4:2:2 BT.656 Embeded Syncs Timing Diagram

Table 11. Single Pixel Mode YCbCr 4:2:2 BT.1120 Pin Mapping

	Single Pixel Mode			
Mode CFG 2	0x01	0x01	0x01	0x01
Mode CFG 1	0x15	0x05	0x06	0x07
Mode CFG 0				
Color Space	CrYCb			
Tag	16-Bit 4:2:2 Mode B	16-Bit 4:2:2 Mode A	20-Bit 4:2:2	24-Bit 4:2:2 Mode A
Standard	BT.1120	BT.1120	BT.1120	BT.1120
SDR Clock Ratio	1x	1x	1x	1x
DDR Clock Ratio	0.5x	0.5x	0.5x	0.5x
PIN NAME				
DPHYB_5N(V23)	Z	Y7	Y9	Y11
DPHYB_5P(V22)	Z	Y6	Y8	Y10
DPHYB_4N(V21)	Z	Y5	Y7	Y9
DPHYB_4P(V20)	Z	Y4	Y6	Y8
DPHYB_3N(V19)	Z	Y3	Y5	Y7
DPHYB_3P(V18)	Z	Y2	Y4	Y6
DPHYB_2N(V17)	Z	Y1	Y3	Y5
DPHYB_2P(V16)	Z	Y0	Y2	Y4
DPHYB_1N(V15)	Y7	Z	Y1	Y3
DPHYB_1P(V14)	Y6	Z	Y0	Y2
DPHYB_0N(V13)	Y5	Z	Z	Y1
DPHYB_0P(V12)	Y4	Z	Z	Y0
DPHYA_5N(V11)	Y3	C7	C9	C11
DPHYA_5P(V10)	Y2	C6	C8	C10
DPHYA_4N(V9)	Y1	C5	C7	C9
DPHYA_4P(V8)	Y0	C4	C6	C8
DPHYA_3N(V7)	C7	C3	C5	C7
DPHYA_3P(V6)	C6	C2	C4	C6
DPHYA_2N(V5)	C5	C1	C3	C5
DPHYA_2P(V4)	C4	C0	C2	C4
DPHYA_1N(V3)	C3	Z	C1	C3
DPHYA_1P(V2)	C2	Z	C0	C2
DPHYA_0N(V1)	C1	Z	Z	C1
DPHYA_0P(V0)	C0	Z	Z	C0
DPHY_VSP(VS)	VS/Embedded	VS/Embedded	VS/Embedded	VS/Embedded
DPHY_HSP(HS)	HS/Embedded	HS/Embedded	HS/Embedded	HS/Embedded
DPHY_DEP(DE)	DE/Embedded	DE/Embedded	DE/Embedded	DE/Embedded

Table 12. Single Pixel Mode YCbCr 4:2:2 BT.656 Pin Mapping

Mode CFG 2	0x02/0x42		0x02/0x42		0x02/0x42		0x02/0x42		0x02/0x42		0x02/0x42		0x02/0x42	
Mode CFG 1	0x05		0x06		0x07		0x11		0x01		0x02		0x03	
Mode CFG 0														
Color Space	YCBCR													
Tag	8-Bit 4:2:2		10-Bit 4:2:2		12-Bit 4:2:2 Mode A		12-Bit 4:4:4 Mode B		12-Bit 4:4:4 Mode A		15-Bit 4:4:4		18-Bit 4:4:4	
Standard	BT. 656		BT. 656		BT. 656									
SDR Clock Ratio	2x		2x		2x		2x		2x		2x		2x	
DDR Clock Ratio	1x		1x		1x		1x		1x		1x		1x	
PIN NAME	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
DPHYB_2N(V17)									Y3	Cr7	Y4	Cr9	Y5	Cr11
DPHYB_2P(V16)									Y2	Cr6	Y3	Cr8	Y4	Cr10
DPHYB_1N(V15)									Y1	Cr5	Y2	Cr7	Y3	Cr9
DPHYB_1P(V14)									Y0	Cr4	Y1	Cr6	Y2	Cr8
DPHYB_0N(V13)									Cb7	Cr3	Y0	Cr5	Y1	Cr7
DPHYB_0P(V12)									Cb6	Cr2	C9	Cr4	Y0	Cr6
DPHYA_5N(V11)	C7	Y7	C9	Y9	C11	Y11	Cr7	Cb7	Cb5	Cr1	C8	Cr3	Cb11	Cr5
DPHYA_5P(V10)	C6	Y6	C8	Y8	C10	Y10	Cr6	Cb6	Cb4	Cr0	C7	Cr2	Cb10	Cr4
DPHYA_4N(V9)	C5	Y5	C7	Y7	C9	Y9	Cr5	Cb5	Cb3	Y7	C6	Cr1	Cb9	Cr3
DPHYA_4P(V8)	C4	Y4	C6	Y6	C8	Y8	Cr4	Cb4	Cb2	Y6	C5	Cr0	Cb8	Cr2
DPHYA_3N(V7)	C3	Y3	C5	Y5	C7	Y7	Cr3	Cb3	Cb1	Y5	C4	Y9	Cb7	Cr1
DPHYA_3P(V6)	C2	Y2	C4	Y4	C6	Y6	Cr2	Cb2	Cb0	Y4	C3	Y8	Cb6	Cr0
DPHYA_2N(V5)	C1	Y1	C3	Y3	C5	Y5	Cr1	Cb1	Z	Z	C2	Y7	Cb5	Y11
DPHYA_2P(V4)	C0	Y0	C2	Y2	C4	Y4	Cr0	Cb0	Z	Z	C1	Y6	Cb4	Y10
DPHYA_1N(V3)	Z	Z	C1	Y1	C3	Y3	Y7	Y3	Z	Z	C0	Y5	Cb3	Y9
DPHYA_1P(V2)	Z	Z	C0	Y0	C2	Y2	Y6	Y2	Z	Z	Z	Z	Cb2	Y8
DPHYA_0N(V1)	Z	Z	Z	Z	C1	Y1	Y5	Y1	Z	Z	Z	Z	Cb1	Y7
DPHYA_0P(V0)	Z	Z	Z	Z	C0	Y0	Y4	Y0	Z	Z	Z	Z	Cb0	Y6
DPHY_VSP(VS)	VS/Embedded		VS/Embedded		VS/Embedded		VS		VS		VS		VS	
DPHY_HSP(HS)	HS/Embedded		HS/Embedded		HS/Embedded		HS		HS		HS		HS	
DPHY_DEP(DE)	DE/Embedded		DE/Embedded		DE/Embedded		DE		DE		DE		DE	
Color Space	RGB													
DPHYB_2N(V17)									G3	R7	G4	R9	G5	R11
DPHYB_2P(V16)									G2	R6	G3	R8	G4	R10
DPHYB_1N(V15)									G1	R5	G2	R7	G3	R9
DPHYB_1P(V14)									G0	R4	G1	R6	G2	R8
DPHYB_0N(V13)									B7	R3	G0	R5	G1	R7
DPHYB_0P(V12)									B6	R2	B9	R4	G0	R6
DPHYA_5N(V11)							R7	B7	B5	R1	B8	R3	B11	R5
DPHYA_5P(V10)							R6	B6	B4	R0	B7	R2	B10	R4
DPHYA_4N(V9)							R5	B5	B3	G7	B6	R1	B9	R3
DPHYA_4P(V8)							R4	B4	B2	G6	B5	R0	B8	R2
DPHYA_3N(V7)							R3	B3	B1	G5	B4	G9	B7	R1
DPHYA_3P(V6)							R2	B2	B0	G4	B3	G8	B6	R0
DPHYA_2N(V5)							R1	B1	Z	Z	B2	G7	B5	G11
DPHYA_2P(V4)							R0	B0	Z	Z	B1	G6	B4	G10
DPHYA_1N(V3)							G7	G3	Z	Z	B0	G5	B3	G9
DPHYA_1P(V2)							G6	G2	Z	Z	Z	Z	B2	G8
DPHYA_0N(V1)							G5	G1	Z	Z	Z	Z	B1	G7
DPHYA_0P(V0)							G4	G0	Z	Z	Z	Z	B0	G6
DPHY_VSP(VS)							VS		VS		VS		VS	
DPHY_HSP(HS)							HS		HS		HS		HS	
DPHY_DEP(DE)							DE		DE		DE		DE	

2.3.2 LVDS Output Mode

In LVDS mode, GSV2725 can support VESA and JEIDA LVDS standard. GSV2725 can support both single pixel and dual pixel mode using LVDS.

The VESA standard color mapping is shown in Figure 8.

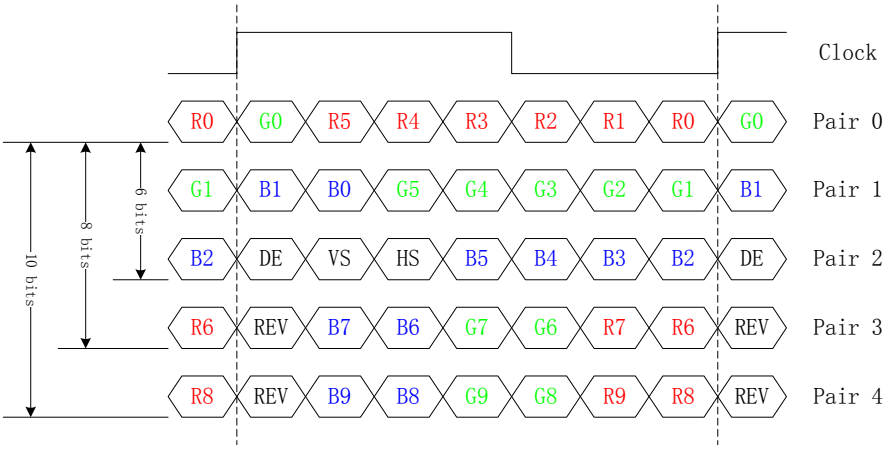


Figure 8. VESA LVDS Color Mapping

The JEIDA standard color mapping is shown in Figure 9.

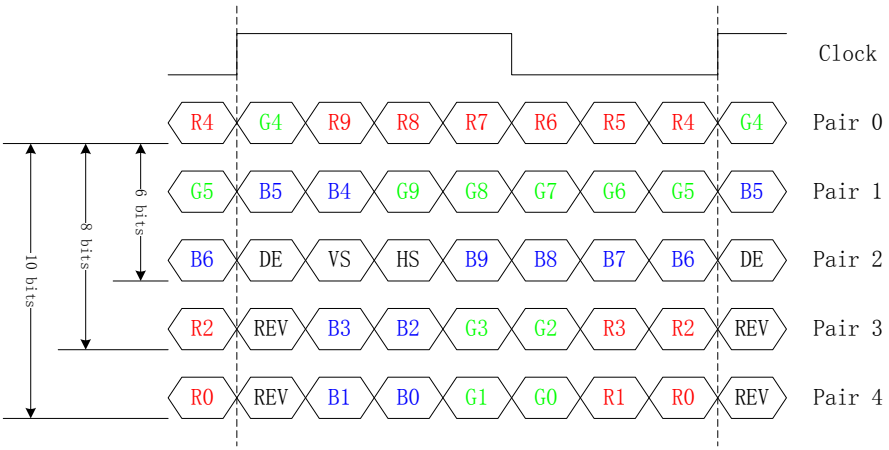


Figure 9. JEIDA LVDS Color Mapping

In GSV2725, LVDS max data rate is 1.2Gbps, for the single pixel VESA or JEIDA port, the max pixel clock frequency is 171MHz. Single pixel mode VESA or JEIDA port can support 1080P60 4:4:4 10-bits. Dual pixel mode VESA or JEIDA ports can support 4K30 4:4:4 10-bits.

Table 13. Single/Dual Pixel Mode LVDS VESA/JEIDA Pin Mapping

Mode CFG 2	0x07														
Mode CFG 1	VESA Single Pixel 6/8/10/12bits -> 0x80/81/82/83							JEDIA Single Pixel 6/8/10/12bits -> 0xC0/C1/C2/C3							
Mode CFG 0															
Color Space	RGB														
Standard	VESA							JEIDA							
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	
DPHYB_5P/N(V11)	CK H	CK H	CK H	CK H	CK L	CK L	CK L	CK H	CK H	CK H	CK H	CK L	CK L	CK L	Dual Pixel
DPHYB_4P/N(V10)	N/A	B9	B8	G9	G8	R9	R8	N/A	B1	B0	G1	G0	R1	R0	
DPHYB_3P/N(V9)	N/A	B7	B6	G7	G6	R7	R6	N/A	B3	B2	G3	G2	R3	R2	
DPHYB_2P/N(V8)	DE	VS	HS	B5	B4	B3	B2	DE	VS	HS	B9	B8	B7	B6	
DPHYB_1P/N(V7)	B1	B0	G5	G4	G3	G2	G1	B5	B4	G9	G8	G7	G6	G5	
DPHYB_0P/N(V6)	G0	R5	R4	R3	R2	R1	R0	G4	R9	R8	R7	R6	R5	R4	
DPHYA_5P/N(V5)	CK H	CK H	CK H	CK H	CK L	CK L	CK L	CK H	CK H	CK H	CK H	CK L	CK L	CK L	Single Pixel
DPHYA_4P/N(V4)	N/A	B9	B8	G9	G8	R9	R8	N/A	B1	B0	G1	G0	R1	R0	
DPHYA_3P/N(V3)	N/A	B7	B6	G7	G6	R7	R6	N/A	B3	B2	G3	G2	R3	R2	
DPHYA_2P/N(V2)	DE	VS	HS	B5	B4	B3	B2	DE	VS	HS	B9	B8	B7	B6	
DPHYA_1P/N(V1)	B1	B0	G5	G4	G3	G2	G1	B5	B4	G9	G8	G7	G6	G5	
DPHYA_0P/N(V0)	G0	R5	R4	R3	R2	R1	R0	G4	R9	R8	R7	R6	R5	R4	

To achieve 4K60 10-bit transmission using LVDS interface, LVDS 5x dual pixel would be required. Max LVDS data rate is 1.5Gbps for 4K60 10-bit. Separate Sync pins can help on timing recovery.

Table 14. Single/Dual Pixel Mode LVDS 5x Pin Mapping

Color Space	CrYCb									
Tag	8-Bit					10-Bit				
Standard										
SDR Clock Ratio	5x					5x				
DDR Clock Ratio	2.5x					2.5x				
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4
DPHYB_5P/N(V11)	Z	Z	Z	Z	Z	Cr5	Cr6	Cr7	Cr8	Cr9
DPHYB_4P/N(V10)	Z	Z	Z	Z	Z	Cr0	Cr1	Cr2	Cr3	Cr4
DPHYB_3P/N(V9)	Cr5	Cr6	Cr7	Z	Z	Y5	Y6	Y7	Y8	Y9
DPHYB_2P/N(V8)	Cr0	Cr1	Cr2	Cr3	Cr4	Y0	Y1	Y2	Y3	Y4
DPHYB_1P/N(V7)	Y3	Y4	Y5	Y6	Y7	Cb5	Cb6	Cb7	Cb8	Cb9
DPHYB_0P/N(V6)	Cb6	Cb7	Y0	Y1	Y2	Cb0	Cb1	Cb2	Cb3	Cb4
DPHYA_5P/N(V5)	Cb1	Cb2	Cb3	Cb4	Cb5	Cr5	Cr6	Cr7	Cr8	Cr9
DPHYA_4P/N(V4)	Cr4	Cr5	Cr6	Cr7	Cb0	Cr0	Cr1	Cr2	Cr3	Cr4
DPHYA_3P/N(V3)	Y7	Cr0	Cr1	Cr2	Cr3	Y5	Y6	Y7	Y8	Y9
DPHYA_2P/N(V2)	Y2	Y3	Y4	Y5	Y6	Y0	Y1	Y2	Y3	Y4
DPHYA_1P/N(V1)	Cb5	Cb6	Cb7	Y0	Y1	Cb5	Cb6	Cb7	Cb8	Cb9
DPHYA_0P/N(V0)	Cb0	Cb1	Cb2	Cb3	Cb4	Cb0	Cb1	Cb2	Cb3	Cb4
DPHY_VS	VS					VS				
DPHY_HS	HS					HS				
DPHY_DE	DE					DE				
Color Space	RGB									
DPHYB_5P/N(V11)	Z	Z	Z	Z	Z	R5	R6	R7	R8	R9
DPHYB_4P/N(V10)	Z	Z	Z	Z	Z	R0	R1	R2	R3	R4
DPHYB_3P/N(V9)	R5	R6	R7	Z	Z	G5	G6	G7	G8	G9
DPHYB_2P/N(V8)	R0	R1	R2	R3	R4	G0	G1	G2	G3	G4
DPHYB_1P/N(V7)	G3	G4	G5	G6	G7	B5	B6	B7	B8	B9
DPHYB_0P/N(V6)	B6	B7	G0	G1	G2	B0	B1	B2	B3	B4
DPHYA_5P/N(V5)	B1	B2	B3	B4	B5	R5	R6	R7	R8	R9
DPHYA_4P/N(V4)	R4	R5	R6	R7	B0	R0	R1	R2	R3	R4
DPHYA_3P/N(V3)	G7	R0	R1	R2	R3	G5	G6	G7	G8	G9
DPHYA_2P/N(V2)	G2	G3	G4	G5	G6	G0	G1	G2	G3	G4
DPHYA_1P/N(V1)	B5	B6	B7	G0	G1	B5	B6	B7	B8	B9
DPHYA_0P/N(V0)	B0	B1	B2	B3	B4	B0	B1	B2	B3	B4
DPHY_VS	VS					VS				
DPHY_HS	HS					HS				
DPHY_DE	DE					DE				

Table 15. Single/Dual Pixel Mode LVDS 5x YCbCr 4:2:2 Pin Mapping

Color Space	CrYCb														
Tag	8-Bit 4:2:2					10-Bit 4:2:2					12-Bit 4:2:2				
Standard															
SDR Clock Ratio	5x					5x					5x				
DDR Clock Ratio	2.5x					2.5x					2.5x				
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4
V11	Z	Z	Z	Z	Z	0	0	0	0	0	Y7	Y8	Y9	Y10	Y11
V10	Z	Z	Z	Z	Z	0	0	0	0	0	Y2	Y3	Y4	Y5	Y6
V9	0	0	0	Z	Z	Y5	Y6	Y7	Y8	Y9	C9	C10	C11	Y0	Y1
V8	0	0	0	0	0	Y0	Y1	Y2	Y3	Y4	C4	C5	C6	C7	C8
V7	Y3	Y4	Y5	Y6	Y7	C5	C6	C7	C8	C9	0	C0	C1	C2	C3
V6	C6	C7	Y0	Y1	Y2	C0	C1	C2	C3	C4	0	0	0	0	0
V5	C1	C2	C3	C4	C5	0	0	0	0	0	0	0	0	0	0
V4	0	0	0	0	C0	0	0	0	0	0	Y8	Y9	Y10	Y11	0
V3	Y7	0	0	0	0	Y5	Y6	Y7	Y8	Y9	Y3	Y4	Y5	Y6	Y7
V2	Y2	Y3	Y4	Y5	Y6	Y0	Y1	Y2	Y3	Y4	C10	C11	Y0	Y1	Y2
V1	C5	C6	C7	Y0	Y1	C5	C6	C7	C8	C9	C5	C6	C7	C8	C9
V0	C0	C1	C2	C3	C4	C0	C1	C2	C3	C4	C0	C1	C2	C3	C4
VS	VS					VS					VS				
HS	HS					HS					HS				
DE	DE					DE					DE				

To achieve 4K60 12-bit transmission using LVDS interface, LVDS 6x dual pixel would be required. Max LVDS data rate is 1.8Gbps for 4K60 12-bit. Separate Sync pins can help on timing recovery.

Table 16. Single/Dual Pixel Mode LVDS 6x Pin Mapping

Color Space	CrYCb																	
Tag	8-Bit						10-Bit						12-Bit					
Standard																		
SDR Clock Ratio	6x						6x						6x					
DDR Clock Ratio	3x						3x						3x					
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5
V11	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Cr6	Cr7	Cr8	Cr9	C10	C11
V10	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5
V9	Z	Z	Z	Z	Z	Z	Cr4	Cr5	Cr6	Cr7	Cr8	Cr9	Y6	Y7	Y8	Y9	Y10	Y11
V8	Z	Z	Z	Z	Z	Z	Y8	Y9	Cr0	Cr1	Cr2	Cr3	Y0	Y1	Y2	Y3	Y4	Y5
V7	Cr2	Cr3	Cr4	Cr5	Cr6	Cr7	Y2	Y3	Y4	Y5	Y6	Y7	Cb6	Cb7	Cb8	Cb9	Cb10	Cb11
V6	Y4	Y5	Y6	Y7	Cr0	Cr1	Cb6	Cb7	Cb8	Cb9	Y0	Y1	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5
V5	Cb6	Cb7	Y0	Y1	Y2	Y3	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cr6	Cr7	Cr8	Cr9	C10	C11
V4	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cr4	Cr5	Cr6	Cr7	Cr8	Cr9	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5
V3	Cr2	Cr3	Cr4	Cr5	Cr6	Cr7	Y8	Y9	Cr0	Cr1	Cr2	Cr3	Y6	Y7	Y8	Y9	Y10	Y11
V2	Y4	Y5	Y6	Y7	Cr0	Cr1	Y2	Y3	Y4	Y5	Y6	Y7	Y0	Y1	Y2	Y3	Y4	Y5
V1	Cb6	Cb7	Y0	Y1	Y2	Y3	Cb6	Cb7	Cb8	Cb9	Y0	Y1	Cb6	Cb7	Cb8	Cb9	Cb10	Cb11
V0	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5
VS	VS						VS						VS					
HS	HS						HS						HS					
DE	DE						DE						DE					
Color Space	RGB																	
V11	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	R6	R7	R8	R9	C10	C11
V10	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	R0	R1	R2	R3	R4	R5
V9	Z	Z	Z	Z	Z	Z	R4	R5	R6	R7	R8	R9	G6	G7	G8	G9	G10	G11
V8	Z	Z	Z	Z	Z	Z	G8	G9	R0	R1	R2	R3	G0	G1	G2	G3	G4	G5
V7	R2	R3	R4	R5	R6	R7	G2	G3	G4	G5	G6	G7	B6	B7	B8	B9	B10	B11
V6	G4	G5	G6	G7	R0	R1	B6	B7	B8	B9	G0	G1	B0	B1	B2	B3	B4	B5
V5	B6	B7	G0	G1	G2	G3	B0	B1	B2	B3	B4	B5	R6	R7	R8	R9	C10	C11
V4	B0	B1	B2	B3	B4	B5	R4	R5	R6	R7	R8	R9	R0	R1	R2	R3	R4	R5
V3	R2	R3	R4	R5	R6	R7	G8	G9	R0	R1	R2	R3	G6	G7	G8	G9	G10	G11
V2	G4	G5	G6	G7	R0	R1	G2	G3	G4	G5	G6	G7	G0	G1	G2	G3	G4	G5
V1	B6	B7	G0	G1	G2	G3	B6	B7	B8	B9	G0	G1	B6	B7	B8	B9	B10	B11
V0	B0	B1	B2	B3	B4	B5	B0	B1	B2	B3	B4	B5	B0	B1	B2	B3	B4	B5
VS	VS						VS						VS					
HS	HS						HS						HS					
DE	DE						DE						DE					

Typical LVDS 4x guarantee 4K60 8-bit transmission in 1.2Gbps using dual pixel.

Table 17. Single/Dual Pixel Mode RGB/YCbCr 4:4:4 LVDS 4x Pin Mapping

	Dual Pixel Mode			
Mode CFG 2	0x14			
Mode CFG 1	0x01			
Mode CFG 0				
Color Space	CrYCb 4:4:4			
Tag	8-Bit 4:4:4			
SDR Clock Ratio	4x			
DDR Clock Ratio	2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0
DPHYB_5P/N(V11)	P1.Cr7	P1.Cr6	P1.Cr5	P1.Cr4
DPHYB_4P/N(V10)	P1.Cr3	P1.Cr2	P1.Cr1	P1.Cr0
DPHYB_3P/N(V9)	P1.Y7	P1.Y6	P1.Y5	P1.Y4
DPHYB_2P/N(V8)	P1.Y3	P1.Y2	P1.Y1	P1.Y0
DPHYB_1P/N(V7)	P1.Cb7	P1.Cb6	P1.Cb5	P1.Cb4
DPHYB_0P/N(V6)	P1.Cb3	P1.Cb2	P1.Cb1	P1.Cb0
DPHYA_5P/N(V5)	P0.Cr7	P0.Cr6	P0.Cr5	P0.Cr4
DPHYA_4P/N(V4)	P0.Cr3	P0.Cr2	P0.Cr1	P0.Cr0
DPHYA_3P/N(V3)	P0.Y7	P0.Y6	P0.Y5	P0.Y4
DPHYA_2P/N(V2)	P0.Y3	P0.Y2	P0.Y1	P0.Y0
DPHYA_1P/N(V1)	P0.Cb7	P0.Cb6	P0.Cb5	P0.Cb4
DPHYA_0P/N(V0)	P0.Cb3	P0.Cb2	P0.Cb1	P0.Cb0
DPHY_VS	VS			
DPHY_HS	HS			
DPHY_DE	DE			
Color Space	RGB			
DPHYB_5P/N(V11)	P1.R7	P1.R6	P1.R5	P1.R4
DPHYB_4P/N(V10)	P1.R3	P1.R2	P1.R1	P1.R0
DPHYB_3P/N(V9)	P1.G7	P1.G6	P1.G5	P1.G4
DPHYB_2P/N(V8)	P1.G3	P1.G2	P1.G1	P1.G0
DPHYB_1P/N(V7)	P1.B7	P1.B6	P1.B5	P1.B4
DPHYB_0P/N(V6)	P1.B3	P1.B2	P1.B1	P1.B0
DPHYA_5P/N(V5)	P0.R7	P0.R6	P0.R5	P0.R4
DPHYA_4P/N(V4)	P0.R3	P0.R2	P0.R1	P0.R0
DPHYA_3P/N(V3)	P0.G7	P0.G6	P0.G5	P0.G4
DPHYA_2P/N(V2)	P0.G3	P0.G2	P0.G1	P0.G0
DPHYA_1P/N(V1)	P0.B7	P0.B6	P0.B5	P0.B4
DPHYA_0P/N(V0)	P0.B3	P0.B2	P0.B1	P0.B0
DPHY_VS	VS			
DPHY_HS	HS			
DPHY_DE	DE			

When using 4:2:2 in LVDS 4x mode, pin mapping is shown below.

Table 18. Single/Dual Pixel Mode RGB/YCbCr 4:2:2 LVDS 4x Pin Mapping

	Dual Pixel Mode											
Mode CFG 2	0x14				0x14				0x14			
Mode CFG 1	0x05				0x06				0x07			
Mode CFG 0												
Color Space	CrYCb 4:2:2											
Tag	8-Bit				10-Bit				12-Bit			
SDR Clock Ratio	4x				4x				4x			
DDR Clock Ratio	2x				2x				2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
DPHYB_5P/N(V11)	Z	Z	Z	Z	Z	Z	Z	Z	P1.Y1	P1.Y0	P1.C1	P1.C0
DPHYB_4P/N(V10)	Z	Z	Z	Z	P1.Y1	P1.Y0	P1.C1	P1.C0	P1.Y3	P1.Y2	P1.C3	P1.C2
DPHYB_3P/N(V9)	P1.Y7	P1.Y6	P1.Y5	P1.Y4	P1.Y9	P1.Y8	P1.Y7	P1.Y6	P1.Y11	P1.Y10	P1.Y9	P1.Y8
DPHYB_2P/N(V8)	P1.Y3	P1.Y2	P1.Y1	P1.Y0	P1.Y5	P1.Y4	P1.Y3	P1.Y2	P1.Y7	P1.Y6	P1.Y5	P1.Y4
DPHYB_1P/N(V7)	P1.C7	P1.C6	P1.C5	P1.C4	P1.C9	P1.C8	P1.C7	P1.C6	P1.C11	P1.C10	P1.C9	P1.C8
DPHYB_0P/N(V6)	P1.C3	P1.C2	P1.C1	P1.C0	P1.C5	P1.C4	P1.C3	P1.C2	P1.C7	P1.C6	P1.C5	P1.C4
DPHYA_5P/N(V5)	Z	Z	Z	Z	Z	Z	Z	Z	P0.Y1	P0.Y0	P0.C1	P0.C0
DPHYA_4P/N(V4)	Z	Z	Z	Z	P0.Y1	P0.Y0	P0.C1	P0.C0	P0.Y3	P0.Y2	P0.C3	P0.C2
DPHYA_3P/N(V3)	P0.Y7	P0.Y6	P0.Y5	P0.Y4	P0.Y9	P0.Y8	P0.Y7	P0.Y6	P0.Y11	P0.Y10	P0.Y9	P0.Y8
DPHYA_2P/N(V2)	P0.Y3	P0.Y2	P0.Y1	P0.Y0	P0.Y5	P0.Y4	P0.Y3	P0.Y2	P0.Y7	P0.Y6	P0.Y5	P0.Y4
DPHYA_1P/N(V1)	P0.C7	P0.C6	P0.C5	P0.C4	P0.C9	P0.C8	P0.C7	P0.C6	P0.C11	P0.C10	P0.C9	P0.C8
DPHYA_0P/N(V0)	P0.C3	P0.C2	P0.C1	P0.C0	P0.C5	P0.C4	P0.C3	P0.C2	P0.C7	P0.C6	P0.C5	P0.C4
DPHY_VS	VS				VS				VS			
DPHY_HS	HS				HS				HS			
DPHY_DE	DE				DE				DE			

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

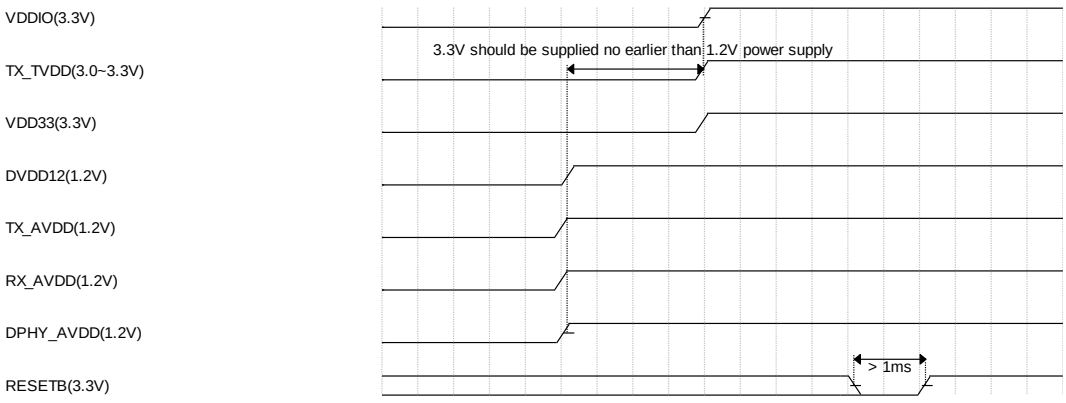


Figure 10. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

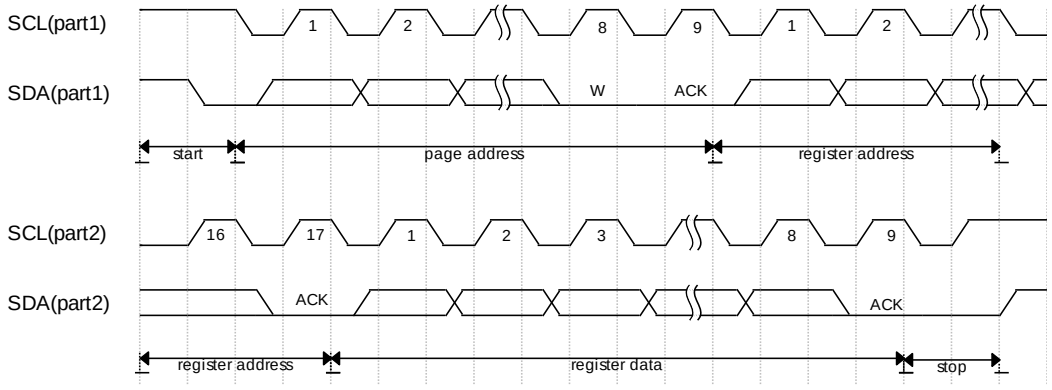


Figure 11. I2C Timing Diagram(Write)

The I2C read timing is shown below.

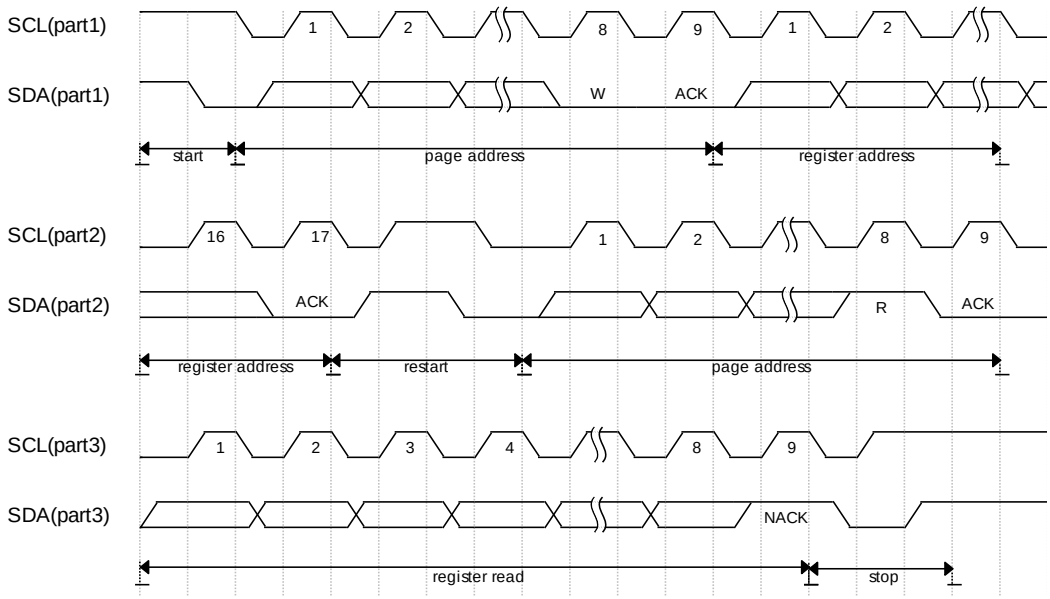


Figure 12. I2C Timing Diagram(Read)

3.1.3 I2S Timing Diagrams

I2S standard timing is shown as below, which is the default I2S timing of audio input/output.

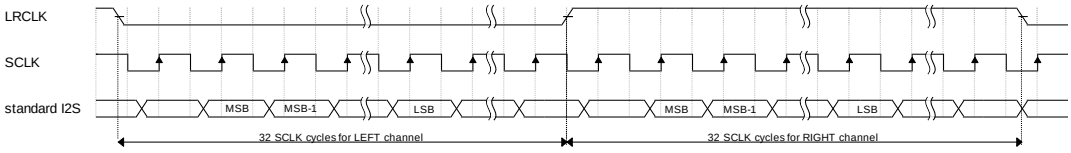


Figure 13. I2S Standard Timing Diagram

I2S left-justified timing is shown as below, which is can be tuned by register configuration.

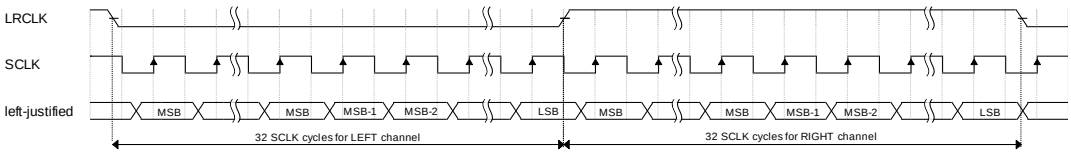


Figure 14. I2S Left-Justified Timing Diagram

I2S right-justified timing is shown as below, which is can be tuned by register configuration.

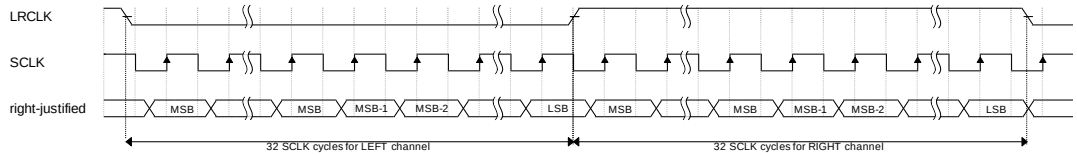


Figure 15. I2S Right-Justified Timing Diagram

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV2725's operation temperature range is -40 ºC to 85 ºC. The maximum junction temperature is at 125 ºC.

3.2.2 Audio Pin Conditions

GSV2725's Audio TTL pin characteristic is the same as other GPIO. By default, Audio pin is TTL push-pull circuit design. Refer to Section 3.2.8 for details.

3.2.3 I2C and SPI Conditions

GSV2725's I2C maximum SCL frequency is 400KHz. GSV2725's I2C behaves as open-drain circuit when VDD33 and VDDIO pins are power supplied. When VDD33 and VDDIO pins are not supplied with power, GSV2725 internal circuit could leak external I2C power to VDD33/VDDIO pins.

Table 19. Recommended SPI Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_C	Serial Clock Frequency	12.5MHz		25	MHz
t_{CLH}	Serial Clock High Time	18	20	40.11	ns
t_{CKL}	Clock low-level width for QSPI	18	20	38.89	ns
t_{CLCH}	Serial Clock Rise Time	0.2	0.63		V/ns
t_{CHCL}	Serial Clock Fall Time	0.2	0.66		V/ns
t_{SLCH}	CS# Active Setup Time	5	60		ns
t_{CHSH}	CS# Active Hold Time	5	104		ns
t_{SHCH}	CS# Not Active Setup Time	5			ns

t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20	98		ns
t_{CLQX}	Output Hold Time	1.2	1.399		ns
t_{DVCH}	Data In Setup Time	2	17		ns
t_{CHDX}	Data In Hold Time	2	22		ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid		4.999	7	ns

Table 20. Recommended I2C Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_{scl}	Clock Cycle for QSPI		300	400	KHz
t_{LOW}	clock low period	1.3	2		us
t_{HIGH}	clock high period	0.6	0.9		us
t_{BUF}	bus free time before new start	1.3			us
$t_{VD:DAT}$	data valid time			0.9	us
$t_{SU:STO}$	set-up time for stop condition	0.6	0.65		us
$t_{HD:DAT}$	data in hold time	0	1		us
$t_{SU:DAT}$	data in setup time	0.1	0.639		us
t_R	rise time		260	300	ns
t_F	fall time		20	300	ns

3.2.4 Absolute Maximum Ratings

Table 21. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Digital power supply	DVDD12	-0.3 to 1.4	V
Interface power supply	VDDIO	-0.3 to 4	V
Analog power supply(RX_AVDD,MIPI_AVDD)	AVDD	-0.3 to 1.4	V

Digital IO power supply	VDD33	-0.3 to 4	V
Operating Temperature Range	To	-40 to +85	℃
Storage Temperature Range	Tstg	-40 to +125	℃
Junction Temperature	Tj	+125	℃

3.2.5 ESD Protection

Table 22. ESD Protection

SYMBOL	PARAMETER	VALUE	UNIT
HBM	HBM for SIO(1) pins (JEDEC JS-001-2023)	8000	V
	HBM for other pins (JEDEC JS-001-2023)	4000	V
CDM	ESD CDM (JEDEC JS-002-2022)	1000	V
LU	Latch-up (JED78F)	200	mA

(1) SIO : Include typeC/DP Interface and MIPI interface pins.

3.2.6 Thermal Information

Table 23. Thermal Information

Parameter (1)(2)(3)	Symbol	Value	Unit
Junction-to-ambient thermal resistance	RθJA	19.27	℃/W
Junction-to-board thermal resistance	RθJB	8.54	℃/W
Junction-to-case(top) thermal resistance	RθJCt	3.39	℃/W
Junction-to-case(bottom) thermal resistance	RθJCb	3.53	℃/W
Junction-to-top characterization parameter	ΨJT	0.5	℃/W
Junction-to-board characterization parameter	ΨJB	8.54	℃/W

(1) Test Result according to the JESD51-14 reference document.

(2) PCB Type: JEDEC high-k (2s2p) as defined in JESD 51-7

(3) PCB Size: 76.2mm×114.3mm×1.6mm

3.2.7 Recommended Operating Conditions

Table 24. Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Pins					
Digital power supply	DVDD12	1.14	1.2	1.26	V
Digital interface IO power supply	VDDIO	3.0	3.3	3.6	V
Analog power supply	AVDD	1.14	1.2	1.26	V

Digital IO power supply	VDD33	3.0	3.3	3.6	V

3.2.8 Electrical Characteristics

Table 25. Electrical Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
DisplayPort Receiver Main-Link DC Electrical Characteristics						
Differential Input Termination	Rin		90		110	Ω
Peak-to-Peak Input Differential Swing	VID	VIN+ - VIN-	100		1400	mV
DisplayPort Receiver Main-Link AC Electrical Characteristics						
Unit Interval for HBR3 (8.1Gbps/lane)	UI_HBR3			123		ps
Unit Interval for HBR2 (5.4Gbps/lane)	UI_HBR2			185		ps
Unit Interval for HBR (2.7Gbps/lane)	UI_HBR			370		ps
Unit Interval for RBR (1.62Gbps/lane)	UI_RBR			617		ps
Down Spread Amplitude	SSC	Support frequency rage of 30~33kHZ	0		0.5	%
Jitter Closed-loop Tracking Bandwidth for HBR3	f_{HBR3}		10			MHz
Jitter Closed-loop Tracking Bandwidth for HBR2	f_{HBR2}		10			MHz
Jitter Closed-loop Tracking Bandwidth for HBR	f_{HBR}		10			MHz
Jitter Closed-loop Tracking Bandwidth for RBR	f_{RBR}		5.4			MHz
DisplayPort Receiver AUX DC Electrical Characteristics						
AUX TX Output Differential Peak-to-Peak Voltage	$V_{diff-tx}$		290		1380	mV
AUX RX Output Differential Peak-to-Peak Voltage	$V_{diff-rx}$		270		1360	mV

AUX termination DC resistance	$V_{aux-term}$			100		Ω
Manchester transaction unit interval	UI		0.4		0.6	us
GPIO & Audio						
Input High level	VIH1		0.7*VDD33			V
Input Low level	VIL1				0.3*VDD33	V
Output High level	VOH1	IOH = -4mA	VDD33-0.4			V
Output Low level	VOL1	IOL = 4mA			0.4	V
DisplayPort HPD (Open-Drain Output) need external 1k pull-up resistor to VDD33						
Output Low level	VOL2	IOL = 4mA			0.4	V
I2C Control (Open-Drain)						
Input High level	VIH1		0.7*VDD33			V
Input Low level	VIL1				0.3*VDD33	V
Low level Open-Drain Output Voltage	VOL3	IOL = 4mA			0.4	V
Input Capacitance	CIN				3	pF
VMON Pin						
ADC for VBUS voltage detect	VMON		0.4		2	V
ResetB Pin						
Chip Reset(Active low) Voltage	VIH-rstb		2.5		VDD33+ 0.3	V
	VIL-rstb		-0.3		0.9	

3.2.9 Electrical Characteristics for Parallel Bus

Table 26. Electrical Characteristics for Parallel Bus (MIPI)

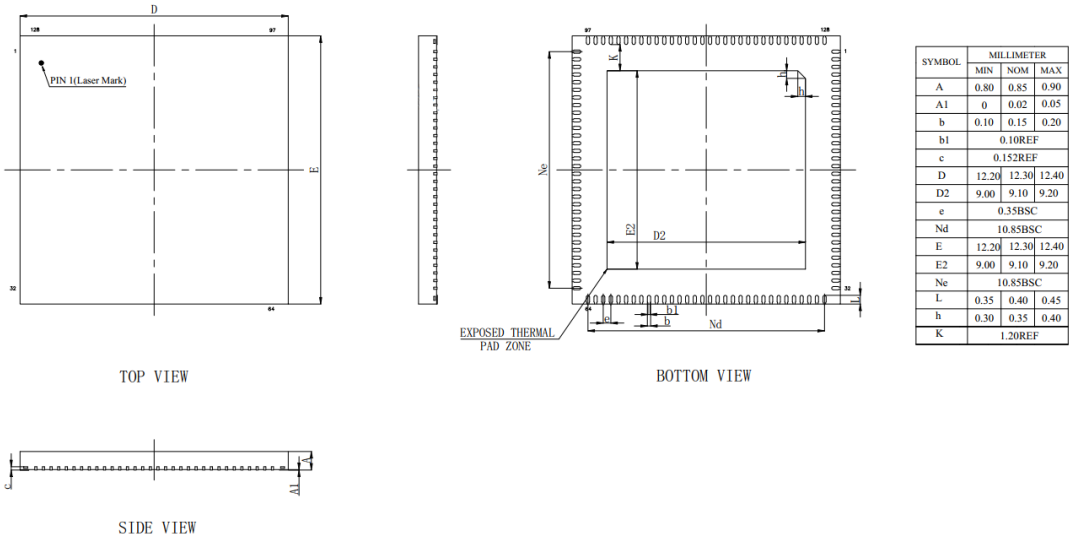
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
MIPI DPHY LP Transmitter DC Electrical Characteristics						
LP output high level output voltage	VOH		0.95	1.2	1.3	V
LP output low level output voltage	VOL		-50		50	mV
Output impedance	ZOLP		110			Ω
MIPI DPHY HS Transmitter DC Electrical Characteristics						
HS transmit static common-mode voltage	VCMTX	ZID = 100Ω	150	220	250	mV
VCMTX Mismatch when Output is differential-1 or differential-0	|△VCMTX(1,0)|	ZID = 100Ω			5	mV

HS transmit differential voltage	|VOD|	ZID = 100Ω	140	180	270	mV
VOD Mismatch when Output is differential-1 or differential-0	|△VOD|	ZID = 100Ω			14	mV
HS output high voltage	VOHHS	ZID = 100Ω			360	mV
Single-ended output impedance	ZOS		40	50	60	Ω
Single-ended output impedance mismatch	△ZOS			10		%
MIPI DPHY LP Transmitter AC Electrical Characteristics						
15% to 85% rise time and fall time	t_{RLP}/t_{FLP}				25	ns
30% to 85% rise time and fall time	t_{REOT}	0-60pF at RX term center tap			35	ns
Load capacitance	C_{LOAD}				70	pF
MIPI DPHY HS Transmitter AC Electrical Characteristics						
Common level variations, HF	$\triangle V_{CMTX}(HF)$	> 450MHz			15	mV_{RMS}
Common level variations, LF	$\triangle V_{CMTX}(LF)$	50MHz to 450MHz			25	mV_{PEAK}
20% to 80% rise time and fall time	t_R and t_F	<1Gbps			0.3	UI
			150			ps
		1 Gbps ~1.5 Gbps			0.35	UI
			100			ps
		>1.5Gbps			0.4	UI
			50			ps
Data lane bit rate	DLBR		80		2500	Mbps
Clock lane frequency	CL_{FREQ}		40		1250	MHz
MIPI DPHY DATA-CLOCK TIMING						
UI instantaneous	UI_{INST}		0.4		12.5	ns
Data to clock skew	t_{SKEW}	80M~ 1.0Gbps	-0.15		0.15	UI_{INST}
		1.0 Gbps~ 1.5Gbps	-0.2		0.2	
Static data to clock skew	t_{SKEW} Static	> 1.5Gbps	-0.2		0.2	UI_{INST}
Dynamic data to clock skew	t_{SKEW} Dynamic	> 1.5Gbps	-0.15		0.15	UI_{INST}

Table 27. Electrical Characteristics for Parallel Bus (LVDS)

Parameter	Symbol	MIN	TYP	MAX	Unit
LVDS DC Electrical Characteristics					
Output differential voltage range	VOD	50		750	mV
Output offset voltage range	VOS	0.9		1.55	V
LVDS AC Electrical Characteristics					
Clock frequency	fclk	25		150	MHz
LVDS data rise time	tR				ns
LVDS data fall time	tF				ns

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1		0.10REF	
c		0.152REF	
D	12.20	12.30	12.40
D2	9.00	9.10	9.20
e		0.35BSC	
Nd		10.85BSC	
E	12.20	12.30	12.40
E2	9.00	9.10	9.20
Ne		10.85BSC	
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		1.20REF	

Figure 16. Package Dimensions (QFN128)

5. Ordering Guide

Table 28. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV2725	−20°C to +85°C	QFN128	Tray

6. Revision History

Table 29. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Jul 3, 2025
V0.2	Add DisplayPort Rx 3D Left/Right Indication Pin	Jul 14, 2025
V0.3	Fix typo of Pin 38/39 description	Aug 26, 2025
V0.4	Update MIPI D-PHY interface characteristic	Dec 3, 2025
V0.5	Add extra pin description for I2C pins	Jan 4, 2026
V0.6	Single/Dual Pixel Mode LVDS 5x YCbCr 4:2:2 Pin Mapping	Apr 1, 2026
V0.7	Declare DSI Tx has no DCS support	Apr 20, 2026

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