GSV5600

DisplayPort 1.4/HDMI 2.1/MIPI/LVDS CAT/Fiber/COAX/Serdes Extender with Embedded MCU

Jan, 2025

Preliminary Product Specification

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TABLES

Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV5600 is a high-performance, low-power DisplayPort 1.4/ HDMI 2.1 CAT/Fiber/COAX/Serdes extender. GSV5600 supports 4K144Hz and 8K60Hz timing in the maximum. Using arbitrarily defined Serdes lane number and lane rate, GSV5600 can support multiple Serdes interfaces, including Fiber/COAX/STP/Ethernet cable. By integrating enhanced microcontroller, GSV5600 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver and DisplayPort Transmitter support up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver and HDMI Transmitter supports up to 48Gbps (FRL, 12G/4Lane). The superior architecture of GSV5600 provides economical smaller footprint solutions using QFN88, targeting for Consumer and ProAV applications.

GSV5600 supports all uncompressed input video/audio decoding/encoding and DSC stream pass-through to output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV5600 for its DisplayPort and HDMI port. HDR-SDR Conversion, Deinterlacer, Downscaler, 444-420 Conversion, Color Space Conversion are supported for flexible video processing. Audio Extraction of HDMI Rx and DisplayPort Rx is supported in GSV5600 for audio processing. Embedded CEC engine enables flexible remote control of the entire HDMI signal chain.

As Serdes extender, internal video codec can be enabled to support up to 8K60Hz 444 format transferred via Fiber/COAX/STP/Ethernet cable. Besides the video and audio transferring through Fiber/COAX/STP/Ethernet cable using Serdes, simultaneous dual direction Infrared, RS232, CEC, USB 1.1 can also be supported by Gscoolink patented technology. When using COAX/STP/Ethernet cable, POE can also be enabled to provide power to the opposite end. GSV5600 Serdes can support up to 12Gbps for fiber module, up to 6Gbps for COAX/STP cable, 1.5Gbps per lane for Ethernet CAT5e/CAT6, 1000BaseTX cable.

By using Gscoolink duplex encoding technology, GSV5600 supports bi-direction USB1.1/CEC/UART/I2C/PWM/GPIO/Infra-Red/SPDIF/I2S/TDM8 protocols. Flexible channel allocation allows customization based on versatile application requirements.

With MIPI CSI-2/LVDS mixed interface, GSV5600 also supports Parallel Bus Interface extension by Serdes. Genuine 4K60 444 can be transmitted using Dual Port MIPI interface. At maximum 2.5Gbps per lane, 4K60 YCbCr 422 can be transmitted using Single Port MIPI interface. LVDS can support 4K30 RGB using Dual Port VESA x7 mode, and 1080P60 RGB using Single Port VESA x7 mode.

Using CAT6 cable in extension, GSV5600 can support 50 meters for 4K144Hz and 8K60Hz extension and 100 meters for 4K60Hz extension.

Within 4kV HBM tolerance, GSV5600's operation temperature range is -40 ºC to 85 ºC.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1 bandwidth, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 4K@60Hz, 4K@30Hz, 480i@60Hz.

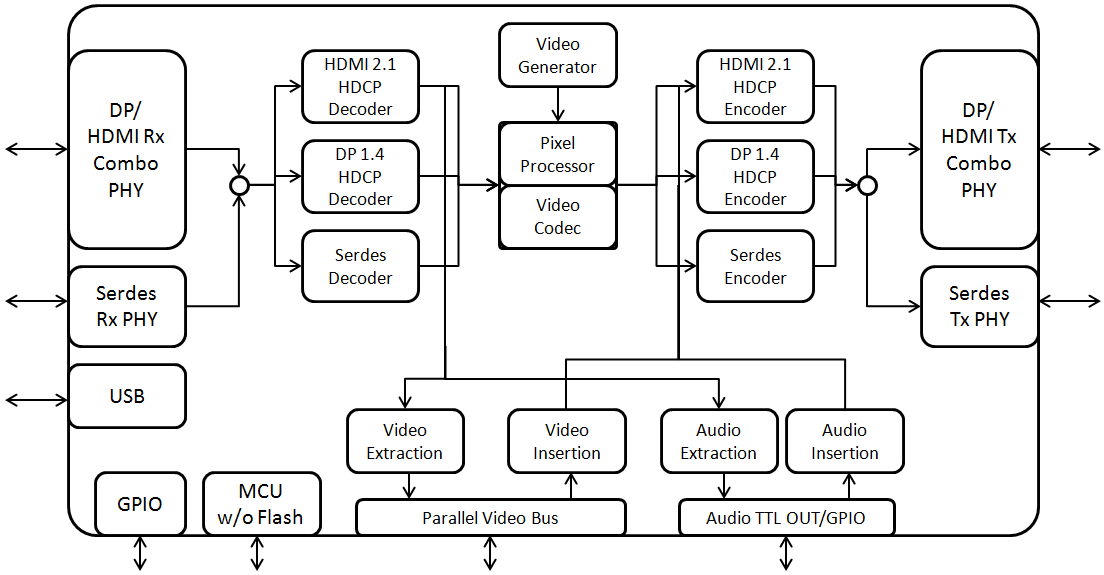


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@120Hz format
- Support Forward Error Correction (FEC)
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support Forward Error Correction (FEC)
- Support DSC pass-through for compressed input timing
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Horizontal Blanking Reduction up to 4K@120Hz format
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.4 HDMI Transmitter

- Compliant with HDMI 2.1a, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support DSC encoded stream pass-through from HDMI/DP input
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.5 Serdes Transceiver

- Support 12Gbps using Fiber Extension
- Support 6Gbps using COAX/STP Extension in maximum 15 meters
- Support 1.5Gbps per lane using Ethernet CAT5e/6 Extension
- Programmable output swing , slew-rate and pre-emphasis
- Support Video/Audio Transmission
- Support up to 6 channel dual-direction duplex transmission
- Support up to 400K baud rate for duplex transmission

1.2.6 Pixel Processor and Video Codec

- HDR to SDR conversion for HDR10, HDR10+, HLG and Low Latency DolbyVision
- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with selectable 2/3/4/8/16/32 ratio
- Deinterlacer for interlaced timing
- Compression/Decompression of up to ratio 16 to lower video stream bandwidth

1.2.7 MIPI CSI-2/DSI-2 Transmitter/Receiver

- Support MIPI CSI-2 v3.0 version transmission using D-PHY or C-PHY interface
- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY In/Out
- Support 5.7G bps 1/2/3-lane MIPI C-PHY Out
- Programmable output swing , slew-rate and pre-emphasis
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.8 Multi-Port LVDS Transmitter/Receiver

- Bi-directional LVDS, supports video format up to 4K60 420 12-bit
  - 4K60 RGB/YCbCr444/YCbCr422 will be converted to YCbCr420
- Compatible with series FPGAs' LVDS standard (12 pairs in maximum)
  - Programmable output swing, slew-rate, common voltage and pre-emphasis
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis

- Data rate up to 1.5Gbps per lane

1.2.9 Audio Output and Input

- TDM8/I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx
- TDM8/I2S and SPDIF Audio Insertion to HDMI Tx/ DisplayPort Tx
- SPDIF/I2S/HBR/DSD/TDM8 Format Supported for Audio Extraction

1.2.10 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 DisplayPort/HDMI to Serdes Conversion

RxPort could be configured as HDMI 2.1 Rx Input. This mode is designed for transmission end of HDMI 2.1 Serdes extension. RxPort could also be configured as DisplayPort Input. This mode is designed for transmission end of DisplayPort Serdes extension.

Using uniform Serdes protocol, regardless of RxPort protocol type of DisplayPort or HDMI Input, TxPort can be configured as DisplayPort or HDMI Output.

When Serdes output is used, DisplayPort/HDMI loop back of transmission end is disabled. Internal Video Codec and Pixel Processor's Color Space Converter, De-Interlacer cannot be used at the same time.

Meanwhile, Video extraction and Audio extraction can be applicable if required.

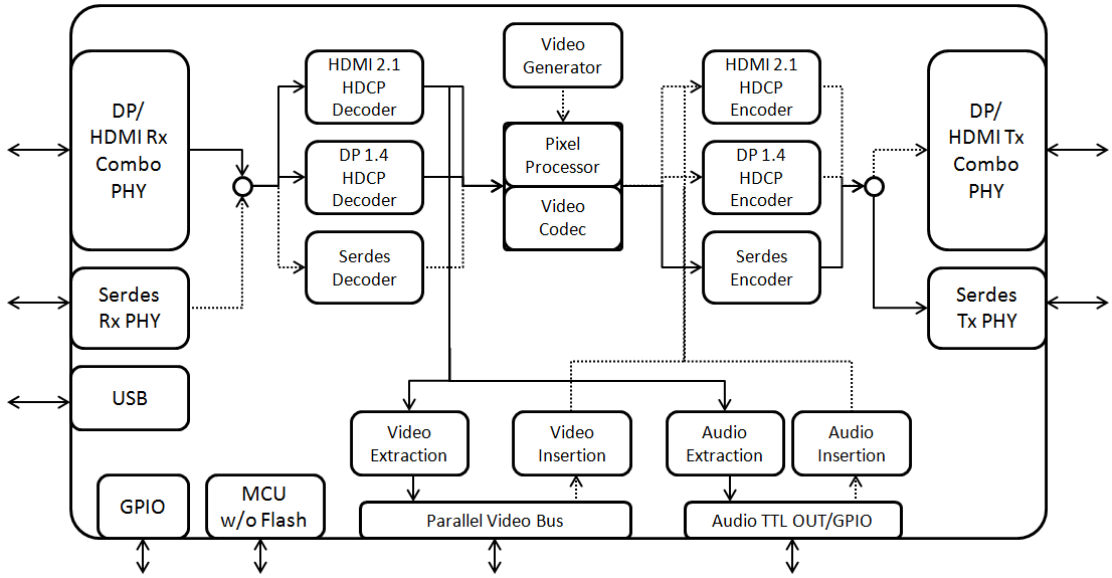


Figure 2. Type-C Alt-Mode/DisplayPort/HDMI to Serdes Application

1.3.2 Serdes to DisplayPort/HDMI Conversion

TxPort could be configured as DisplayPort Tx Output. This mode is designed for reception end of DisplayPort Serdes extension. TxPort could also be configured as HDMI 2.1 Output. This mode is designed for reception end of HDMI Serdes extension.

When Serdes input is used, DisplayPort/HDMI input are disabled. Internal Video Codec and Pixel Processor's Color Space Converter, De-Interlacer cannot be used at the same time. Cascading of GSV5600 is not supported.

Meanwhile, Video extraction and Audio extraction can be applicable if required.

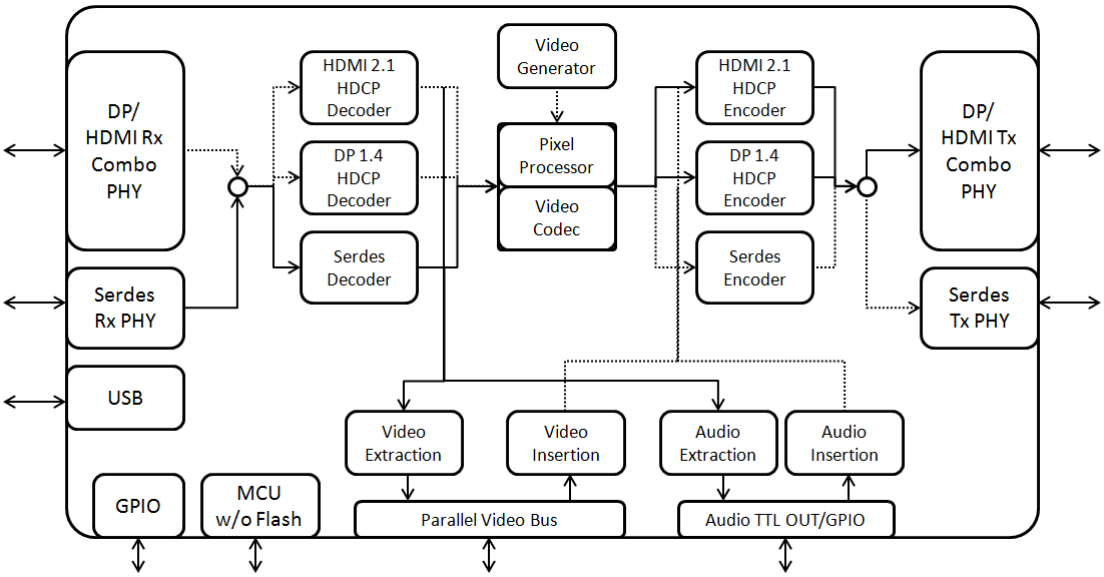


Figure 3. Serdes to DisplayPort/HDMI Application

1.3.3 Serdes Transparent Pass-through pin allocation

There are total 6 forward direction and 6 reverse direction transparent pass-through pins for application use. By default, all the transparent pass-through pins are push-pull configurable input/output. If required, all the transparent pass-through pins can also be configured as open-drain mode.

All AUD1/AUD2 pins are customizable for transparent pass-through use. Each pin can support up to maximum 400 Kbps. By using Gscoolink duplex encoding technology, GSV5600 supports bi-direction UART/I2C/PWM/GPIO/Infra-Red/SPDIF/I2S/TDM8 protocols. Flexible channel allocation allows customization based on versatile application requirements.

A typical transparent pass-through application pin allocation is provided below.

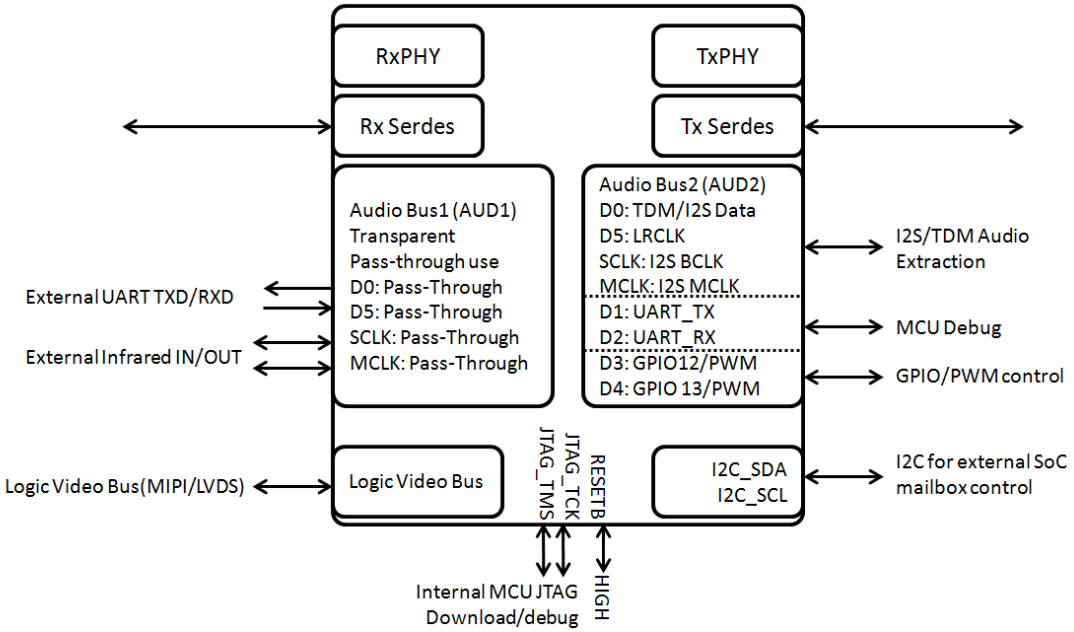


Figure 4. Typical Transparent Pass-through Pin Allocation

1.3.4 Ethernet Transmission Application

When using Ethernet CAT cable transmission, there are 2 options based on application. If there is a need for I2S/TDM8 audio return channel, the following pin connection is needed to support return channel Serdes. 3 differential pairs are configured in forward direction and 1 differential pair is configured in reverse direction. The maximum forward bandwidth is 4.5Gbps, and internal compression engine can compress input video to higher ratio to match the bandwidth.

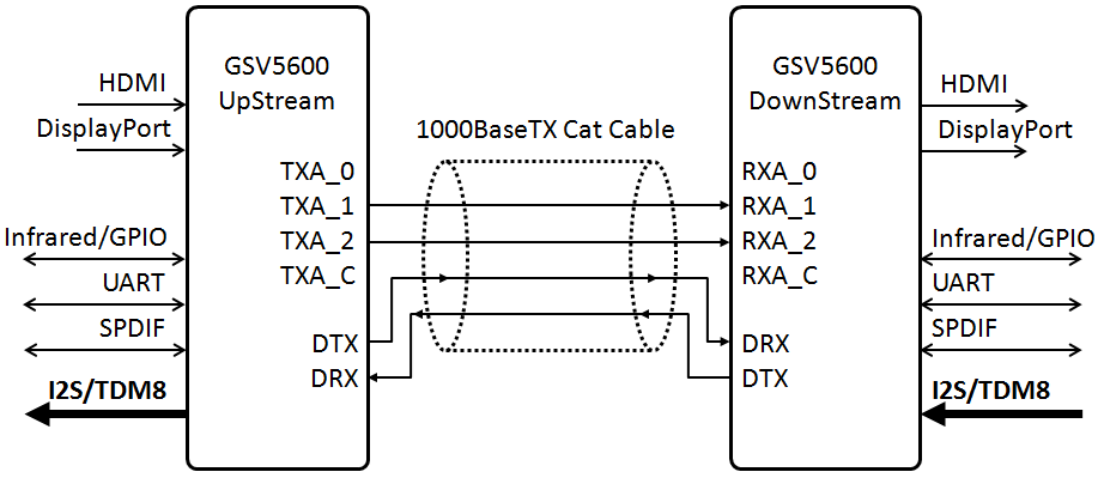


Figure 5. Typical Ethernet Transmission with I2S/TDM8 audio return

If I2S/TDM8 audio return channel is not required, 4 differential pairs can be connected to the same forward direction. The maximum forward bandwidth is 6 Gbps, and internal

compression engine can compress input video to lower ratio to match the bandwidth.

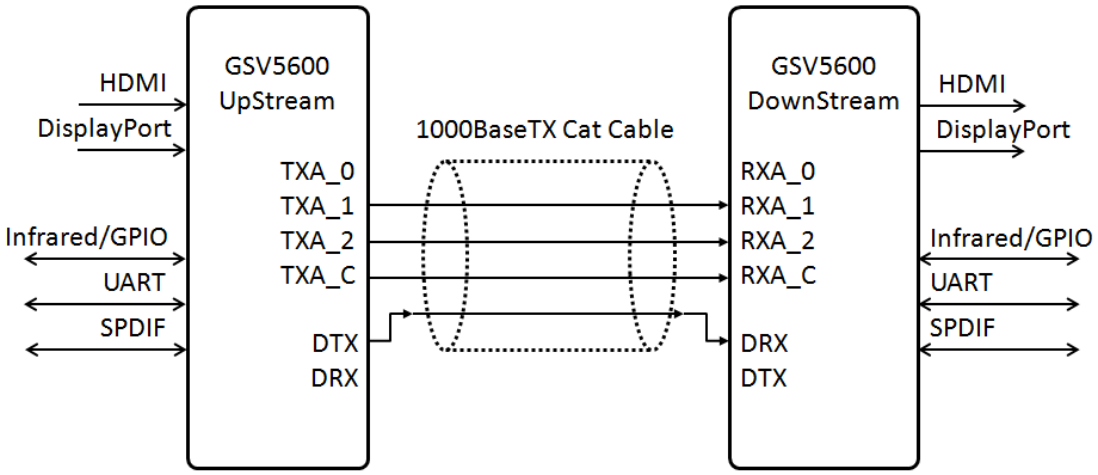


Figure 6. Typical Ethernet Transmission with no I2S/TDM8 audio return

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF needs to be muxed as output. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels SPDIF Data when output is SPDIF
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right) using I2S
SCLK	BCLK	Output	Fixed to 64Fs using I2S
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs using I2S

For TDM format, a fixed format of TDM-8 can be enabled. The Format is listed as below.

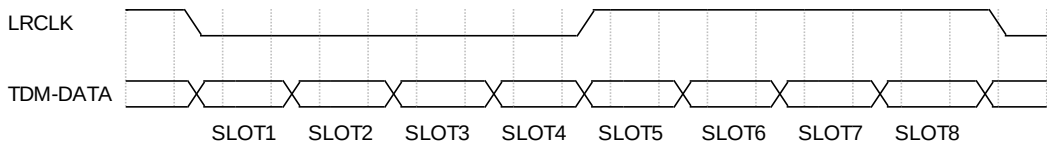


Figure 7. TDM-8 Format

Table 3. TDM Audio Extraction Format

Slot Name	LPCM 2.0 Audio	LPCM 5.1 Audio	LPCM 7.1 Audio
SLOT1	Stereo L	5.1-L	7.1-L

SLOT2	Stereo R	5.1-R	7.1-R
SLOT3		5.1-C	7.1-C
SLOT4		5.1-LFE	7.1-LFE
SLOT5		5.1-LS	7.1-LS
SLOT6		5.1-RS	7.1-RS
SLOT7			7.1-LRS
SLOT8			7.1-RRS

1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode. For SPDIF input, GSV5600 can detect Sampling Frequency and automatically update it in Channel Status in GSV software. For I2S input, software designer needs to indicate the input sampling frequency in GSV software.

Table 4. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 5. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

2. Pin Description

2.1 Pin Diagram

QFN96 Pin definition is defined as below.

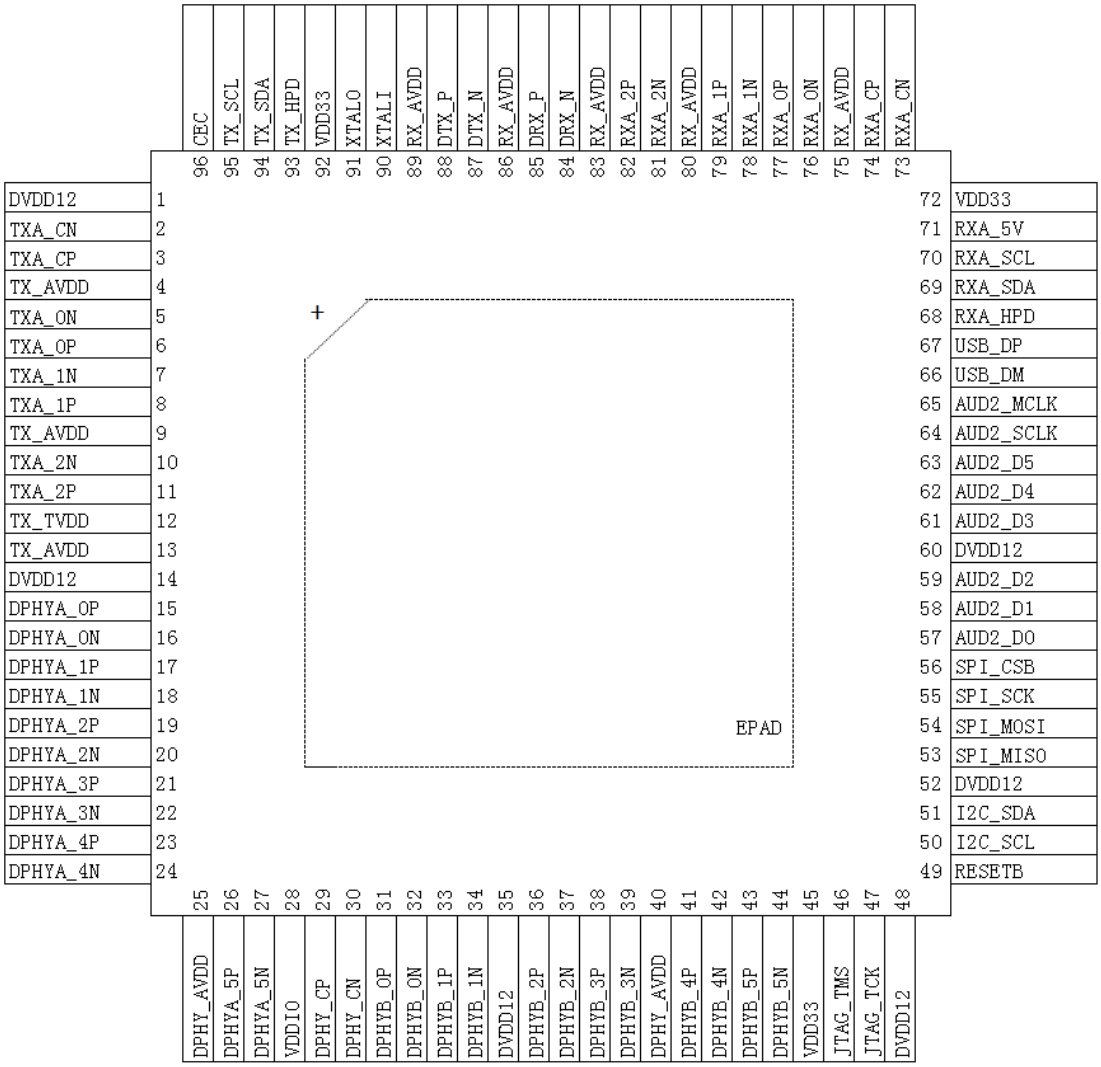


Figure 8. GSV5600 QFN96 Pin Diagram

2.2 QFN96 Pin Description

Table 6. QFN96 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RX Pins/DisplayPort RX Pins			
RXA_5V	I	71	HDMI: RX 5V Detection PAD DP: RX DP Detection PAD

RXA_HPD	O	68	HDMI: RX HPD PAD DP: RX HPD PAD
RXA_SDA	I/O	69	HDMI: RX DDC SDA PAD DP: RX AUX_P PAD
RXA_SCL	I/O	70	HDMI: RX DDC SCL PAD DP: RX AUX_N PAD
RXA_CN	I	73	HDMI: RX Negative TMDS clock differential input DP: RX Negative Main-Link differential data input [0]
RXA_CP	I	74	HDMI: RX Positive TMDS clock differential input DP: RX Positive Main-Link differential data input [0]
RXA_0N	I	76	HDMI: RX Negative TMDS differential data input [0] DP: RX Negative Main-Link differential data input [1]
RXA_0P	I	77	HDMI: RX Positive TMDS differential data input [0] DP: RX Positive Main-Link differential data input [1]
RXA_1N	I	78	HDMI: RX Negative TMDS differential data input [1] DP: RX Negative Main-Link differential data input [2]
RXA_1P	I	79	HDMI: RX Positive TMDS differential data input [1] DP: RX Positive Main-Link differential data input [2]
RXA_2N	I	81	HDMI: RX Negative TMDS differential data input [2] DP: RX Negative Main-Link differential data input [3]
RXA_2P	I	82	HDMI: RX Positive TMDS differential data input [2] DP: RX Positive Main-Link differential data input [3]
Serdes Pins			
DRX_N	I/O	84	Serdes: RX Negative input
DRX_P	I/O	85	Serdes: RX Positive input
DTX_N	I/O	87	Serdes: TX Negative output
DTX_P	I/O	88	Serdes: TX Positive output
HDMI TX Pins/ Type-C DFP/DisplayPort TX Pins			
TXA_SDA	I/O	94	HDMI: TXA DDC SDA PAD DP: TXA AUX_P PAD
TXA_SCL	O	95	HDMI: TXA DDC SCL PAD DP: TXA AUX_N PAD
TXA_HPD	I	93	HDMI: TXA HPD PAD DP: TXA HPD PAD
CEC	I/O	96	TXA CEC Pin
TXA_CN	I/O	2	HDMI: TXA Negative TMDS clock differential output DP: TXA Negative Main-Link differential data output [3]

TXA_CP	I/O	3	HDMI: TXA Positive TMDS clock differential output DP: TXA Positive Main-Link differential data output [3]
TXA_0N	I/O	5	HDMI: TXA Negative TMDS differential data output [0] DP: TXA Negative Main-Link differential data output [2]
TXA_0P	I/O	6	HDMI: TXA Positive TMDS differential data output [0] DP: TXA Positive Main-Link differential data output [2]
TXA_1N	I/O	7	HDMI: TXA Negative TMDS differential data output [1] DP: TXA Negative Main-Link differential data output [1]
TXA_1P	I/O	8	HDMI: TXA Positive TMDS differential data output [1] DP: TXA Positive Main-Link differential data output [1]
TXA_2N	I/O	10	HDMI: TXA Negative TMDS differential data output [2] DP: TXA Negative Main-Link differential data output [0]
TXA_2P	I/O	11	HDMI: TXA Positive TMDS differential data output [2] DP: TXA Positive Main-Link differential data output [0]
Power/Ground Pins			
DVDD12	Power	1,14, 35,48, 52,60,	Digital 1.2V voltage power supply
VDDIO	Power	28	Digital IO 3.3V voltage power supply
DPHY_AVDD	Power	25,40,	Analog 1.2V voltage power supply for Parallel Port
VDD33	Power	45,72, 92	Analog/Digital 3.3V voltage power supply
TX_TVDD	Power	12	Analog 3.3V voltage power supply for TX Port
RX_AVDD	Power	75,80, 83,86, 89,	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	4,9,13	Analog 1.2V voltage power supply for TX Port
MIPI Tx Pins			
DPHY_CP	I/O	29	LVDS: LVDS clock differential positive output
DPHY_CN	I/O	30	LVDS: LVDS clock differential negative output
DPHYA_0P	I/O	15	MIPI: PORTA D-PHY Data[0] differential positive output MIPI: PORTA C-PHY Data[0]-A output LVDS: Video In/Out, Positive LVDS Data[0] VESA: PORTA Positive LVDS Data[0] Alternate: Digital IO PAD as GPIO0

DPHYA_0N	I/O	16	MIPI: PORTA D-PHY Data[0] differential negative output MIPI: PORTA C-PHY Data[0]-B output LVDS: Video In/Out, Negative LVDS Data[0] VESA: PORTA Negative LVDS Data[0] Alternate: Digital IO PAD as GPIO1
DPHYA_1P	I/O	17	MIPI: PORTA D-PHY Data[1] differential positive output MIPI: PORTA C-PHY Data[0]-C output LVDS: Video In/Out, Positive LVDS Data[1] VESA: PORTA Positive LVDS Data[1] Alternate: Digital IO PAD as GPIO2
DPHYA_1N	I/O	18	MIPI: PORTA D-PHY Data[1] differential negative output MIPI: PORTA C-PHY Data[1]-A output LVDS: Video In/Out, Negative LVDS Data[1] VESA: PORTA Negative LVDS Data[1] Alternate: Digital IO PAD as GPIO3
DPHYA_2P	I/O	19	MIPI: PORTA D-PHY clock differential positive output MIPI: PORTA C-PHY Data[1]-B output LVDS: Video In/Out, Positive LVDS Data[2] VESA: PORTA Positive LVDS Clock Alternate: Digital IO PAD as GPIO4
DPHYA_2N	I/O	20	MIPI: PORTA D-PHY clock differential negative output MIPI: PORTA C-PHY Data[1]-C output LVDS: Video In/Out, Negative LVDS Data[2] VESA: PORTA Negative LVDS Clock Alternate: Digital IO PAD as GPIO5
DPHYA_3P	I/O	21	MIPI: PORTA D-PHY Data[2] differential positive output MIPI: PORTA C-PHY Data[2]-A output LVDS: Video In/Out, Positive LVDS Data[3] VESA: PORTA Positive LVDS Data[2] Alternate: Digital IO PAD as GPIO6
DPHYA_3N	I/O	22	MIPI: PORTA D-PHY Data[2] differential negative output MIPI: PORTA C-PHY Data[2]-B output LVDS: Video In/Out, Negative LVDS Data[3] VESA: PORTA Negative LVDS Data[2] Alternate: Digital IO PAD as GPIO7

DPHYA_4P	I/O	23	MIPI: PORTA D-PHY Data[3] differential positive output MIPI: PORTA C-PHY Data[2]-C output LVDS: Video In/Out, Positive LVDS Data[4] VESA: PORTA Positive LVDS Data[3] Alternate: Digital IO PAD as GPIO10
DPHYA_4N	I/O	24	MIPI: PORTA D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[4] VESA: PORTA Negative LVDS Data[3] Alternate: Digital IO PAD as GPIO11
DPHYA_5P	I/O	26	LVDS: Video In/Out, Positive LVDS Data[5] VESA: PORTA Positive LVDS Data[4] Alternate: Digital IO PAD as GPIO12
DPHYA_5N	I/O	27	LVDS: Video In/Out, Negative LVDS Data[5] VESA: PORTA Negative LVDS Data[4] Alternate: Digital IO PAD as GPIO13
DPHYB_0P	I/O	31	MIPI: PORTB D-PHY Data[0] differential positive output MIPI: PORTB C-PHY Data[0]-A output LVDS: Video In/Out, Positive LVDS Data[6] VESA: PORTB Positive LVDS Data[0] Alternate: Digital IO PAD as GPIO0
DPHYB_0N	I/O	32	MIPI: PORTB D-PHY Data[0] differential negative output MIPI: PORTB C-PHY Data[0]-B output LVDS: Video In/Out, Negative LVDS Data[6] VESA: PORTB Negative LVDS Data[0] Alternate: Digital IO PAD as GPIO1
DPHYB_1P	I/O	33	MIPI: PORTB D-PHY Data[1] differential positive output MIPI: PORTB C-PHY Data[0]-C output LVDS: Video In/Out, Positive LVDS Data[7] VESA: PORTB Positive LVDS Data[1] Alternate: Digital IO PAD as GPIO2
DPHYB_1N	I/O	34	MIPI: PORTB D-PHY Data[1] differential negative output MIPI: PORTB C-PHY Data[1]-A output LVDS: Video In/Out, Negative LVDS Data[7] VESA: PORTB Negative LVDS Data[1] Alternate: Digital IO PAD as GPIO3

DPHYB_2P	I/O	36	MIPI: PORTB D-PHY clock differential positive output MIPI: PORTB C-PHY Data[1]-B output LVDS: Video In/Out, Positive LVDS Data[8] VESA: PORTB Positive LVDS Clock Alternate: Digital IO PAD as GPIO4
DPHYB_2N	I/O	37	MIPI: PORTB D-PHY clock differential negative output MIPI: PORTB C-PHY Data[1]-C output LVDS: Video In/Out, Negative LVDS Data[8] VESA: PORTB Negative LVDS Clock Alternate: Digital IO PAD as GPIO5
DPHYB_3P	I/O	38	MIPI: PORTB D-PHY Data[2] differential positive output MIPI: PORTB C-PHY Data[2]-A output LVDS: Video In/Out, Positive LVDS Data[9] VESA: PORTB Positive LVDS Data[2] Alternate: Digital IO PAD as GPIO6
DPHYB_3N	I/O	39	MIPI: PORTB D-PHY Data[2] differential negative output MIPI: PORTB C-PHY Data[2]-B output LVDS: Video In/Out, Negative LVDS Data[9] VESA: PORTB Negative LVDS Data[2] Alternate: Digital IO PAD as GPIO7
DPHYB_4P	I/O	41	MIPI: PORTB D-PHY Data[3] differential positive output MIPI: PORTB C-PHY Data[2]-C output LVDS: Video In/Out, Positive LVDS Data[10] VESA: PORTB Positive LVDS Data[3] Alternate: Digital IO PAD as GPIO10
DPHYB_4N	I/O	42	MIPI: PORTB D-PHY Data[3] differential negative output LVDS: Video In/Out, Negative LVDS Data[10] VESA: PORTB Negative LVDS Data[3] Alternate: Digital IO PAD as GPIO11
DPHYB_5P	I/O	43	LVDS: Video In/Out, Positive LVDS Data[11] VESA: PORTB Positive LVDS Data[4] Alternate: Digital IO PAD as GPIO12
DPHYB_5N	I/O	44	LVDS: Video In/Out, Negative LVDS Data[11] VESA: PORTB Negative LVDS Data[4] Alternate: Digital IO PAD as GPIO13
Digital pins			

I2C_SDA	I/O	51	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU
I2C_SCL	I/O	50	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU
AUD2_SCLK	I/O	64	Digital IO PAD Default: SCLK of Audio Bus 2 Alternate 1: GPIO5 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_MCLK	I/O	65	Digital IO PAD Default: MCLK of Audio Bus 2 Alternate 1: GPIO4 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_D0	I/O	57	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: GPIO7 for internal MCU control Alternate 2: UART_TX for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_D1	I/O	58	Digital IO PAD Default: Data1of Audio Bus 2 Alternate 1: GPIO10 for internal MCU control Alternate 2: UART_TX for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_D2	I/O	59	Digital IO PAD Default: Data2 of Audio Bus 2 Alternate 1: GPIO11 for internal MCU control Alternate 2: UART_RX for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_D3	I/O	61	Digital IO PAD Default: Data3 of Audio Bus 2 Alternate 1: GPIO12 for internal MCU control Alternate 2: Advanced Timer1 for internal MCU control Alternate 3: Transparent pass-through input/output

AUD2_D4	I/O	62	Digital IO PAD Default: Data4 of Audio Bus 2 Alternate 1: GPIO13 for internal MCU control Alternate 2: Advanced Timer2 for internal MCU control Alternate 3: Transparent pass-through input/output
AUD2_D5	I/O	63	Digital IO PAD Default: Data5 of Audio Bus 2 Alternate 1: GPIO6 for internal MCU control Alternate 2: UART_RX for internal MCU control Alternate 3: CEC Alternate 4: Transparent pass-through input/output
RESETB	I	49	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	90	25M Crystal Input
XTALO	I/O	91	25M Crystal output
JTAG_TMS	I/O	46	TMS, Internal MCU programming pin
JTAG_TCK	I	47	TCK, Internal MCU programming pin
SPI_SCK	I/O	55	QSPI_SCK for QSPI Flash connection
SPI_CSB	I/O	56	QSPI_CSB for QSPI Flash connection
SPI_MISO	I/O	53	QSPI_MISO for QSPI Flash connection
SPI_MOSI	I/O	54	QSPI_MOSI for QSPI Flash connection
USB_DP	I/O	67	USB 2.0 D+ Pin
USB_DM	I/O	66	USB 2.0 D- Pin

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

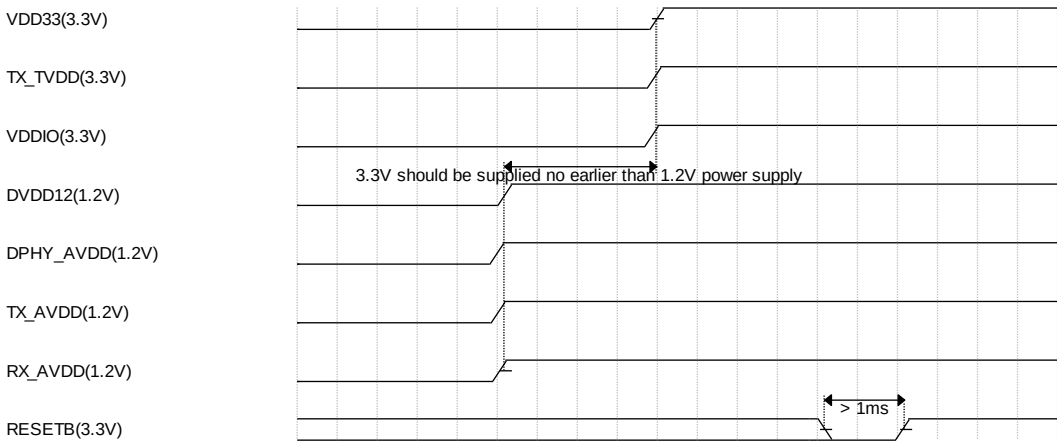


Figure 9. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

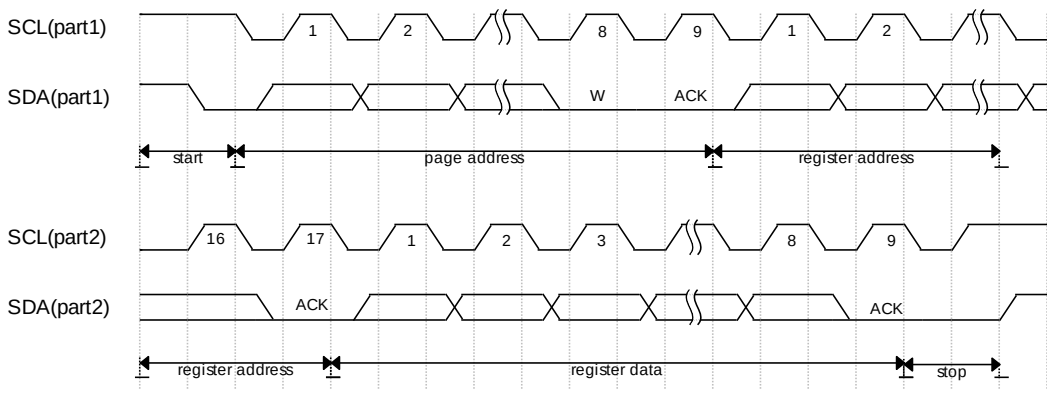


Figure 10. I2C Timing Diagram(Write)

The I2C read timing is shown below.

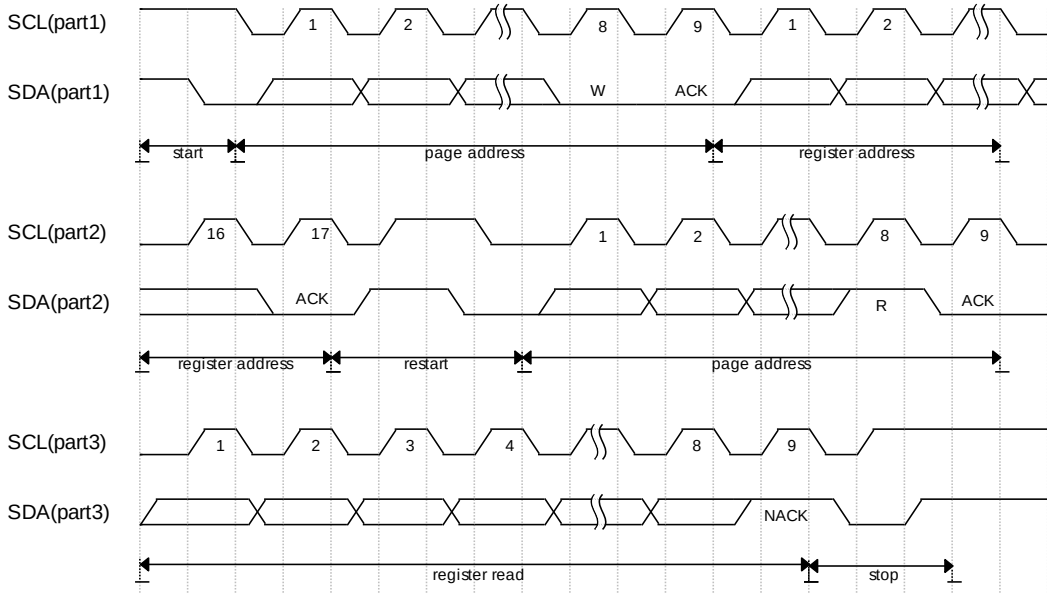


Figure 11. I2C Timing Diagram(Read)

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV5600's operation temperature range is -40 ºC to 85 ºC. The maximum junction temperature is at 125 ºC.

3.2.2 Audio Pin Conditions

GSV5600's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.2.3 I2C and SPI Conditions

GSV5600's I2C maximum SCL frequency is 400KHz.

Table 7. Recommended SPI Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_C	Serial Clock Frequency	12.5MHz		25	MHz
t_{CLH}	Serial Clock High Time	18	20	40.11	ns
t_{CKL}	Clock low-level width for QSPI	18	20	38.89	ns
t_{CLCH}	Serial Clock Rise Time	0.2	0.63		V/ns
t_{CHCL}	Serial Clock Fall Time	0.2	0.66		V/ns
t_{SLCH}	CS# Active Setup Time	5	60		ns
t_{CHSH}	CS# Active Hold Time	5	104		ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20	98		ns
t_{CLQX}	Output Hold Time	1.2	1.399		ns
t_{DVCH}	Data In Setup Time	2	17		ns
t_{CHDX}	Data In Hold Time	2	22		ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns

t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid		4.999	7	ns

Table 8. Recommended I2C Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_{scl}	Clock Cycle for QSPI		300	400	KHz
t_{LOW}	clock low period	1.3	2		us
t_{HIGH}	clock high period	0.6	0.9		us
t_{BUF}	bus free time before new start	1.3			us
$t_{VD:DAT}$	data valid time			0.9	us
$t_{SU:STO}$	set-up time for stop condition	0.6	0.65		us
$t_{HD:DAT}$	data in hold time	0	1		us
$t_{SU:DAT}$	data in setup time	0.1	0.639		us
t_R	rise time		260	300	ns
t_F	fall time		20	300	ns

3.2.4 Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Digital power supply	DVDD12	-0.3 to 1.4	V
Interface power supply	TX_TVDD	-0.3 to 4	V
Analog power supply (RX_AVDD, TX_AVDD, DPHY_AVDD)	AVDD	-0.3 to 1.4	V
Digital IO power supply (VDD33, VDDIO)	VDD33	-0.3 to 4	V
Operating Temperature Range	To	-40 to +85	℃
Storage Temperature Range	Tstg	-40 to +125	℃
Junction Temperature	Tj	+125	℃

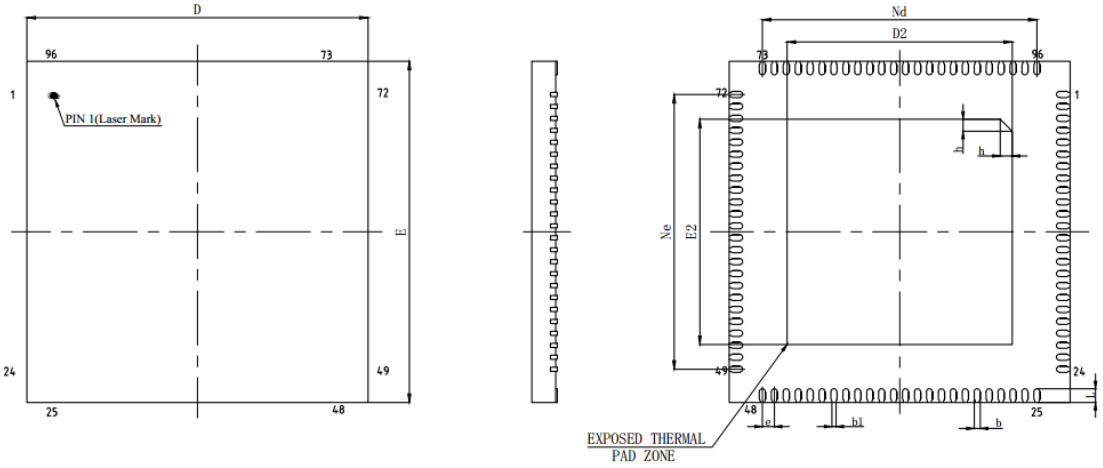
3.2.5 ESD Protection

Table 10. ESD Protection

SYMBOL	PARAMETER	VALUE	UNIT
HBM	HBM for SIO(1) pins (JEDEC JS-001-2023)	8000	V
	HBM for other pins (JEDEC JS-001-2023)	4000	V
CDM	ESD CDM (JEDEC JS-002-2022)	1000	V
LU	Latch-up (JED78F)	200	mA

(1) SIO : Include typeC/DP Interface and MIPI interface pins.

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.18	0.20	0.25
D	9.90	10.0	10.10
D2	6.50	6.60	6.70
e	0.35BSC		
Nd	8.05BSC		
E	9.90	10.0	10.10
E2	6.50	6.60	6.70
Ne	8.05BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 12. Package Dimensions (QFN96)

5. Ordering Guide

Table 11. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV5600	-40°C to +85°C	QFN96	Tray

6. Revision History

Table 12. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Feb 6, 2025
V0.2	Correct GPIO using MIPI pin allocation, add VESA pin allocation description	Aug 18, 2025
V0.3	Update CEC/USB/DSC related information.	Oct 29, 2025
V0.4	Remove typo of eARC description	Nov 7, 2025

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