# GSV5800

Type-C/DisplayPort 1.4/HDMI 2.0 Serdes Extender with Embedded MCU

Oct, 2022

## Preliminary Product Specification

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# Glossary

| | |
|---|---|
| DDC | Display Data Channel |
| EDID | Extended Display Identification Data |
| ESD | Electrostatic Discharge |
| HDCP | High-bandwidth Digital Content Protection |
| HDMI | High-Definition Multimedia Interface |
| HPD | Hot Plug Detect |
| I²C | Inter-Integrated Circuit |
| MCU | Microcontroller Unit |
| MISO | Master In Slave Out |
| MOSI | Master Out Slave In |
| OTP | One Time Programmable |
| PCM | Pulse Code Modulation |
| S/PDIF | Sony/Philips Digital Interface Format |
| SPI | Serial Peripheral Interface |
| TMDS | Transition Minimized Differential Signaling |
| SCDC | Status and Control Data Channel |
| CEC | Consumer Electronics Control |
| AUX | AUX_CH, DisplayPort Auxiliary Channel |
| DPCD | DisplayPort Configuration Data |
| Main-Link | Unidirectional channel stream from DPTX to DPRX |
| SDP | Secondary-data Packet |
| DDC/CI | VESA Display Data Channel/Command Interface |
| MCCS | Monitor Control Command Set (VESA) |
| DP | DisplayPort (VESA) |
| DPRX | DisplayPort Receiver |
| DPTX | DisplayPort Transmitter |
| DSC | Display Stream Compression |
| FEC | Forward Error Correction |
| HBR | DisplayPort High Bit Rate, HDMI High Bit-Rate Audio |
| MST | DisplayPort Multi-Stream Transport |
| SSC | Spread-Spectrum Clock |

# 1. General Description

## 1.1 General Information

Gscoolink GSV5800 is a high-performance, low-power DisplayPort 1.4/ HDMI 2.0 Serdes extender. By integrating enhanced microcontroller, GSV5800 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver supports up to 18Gbps (TMDS, 6G/3Lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV5800 can support Type-C Alternate DisplayPort Serdes extender application. The superior architecture of GSV5800 provides economical smaller footprint solutions using QFN76, targeting for low power embedded applications.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV5800 for its DisplayPort and HDMI port. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Extraction of HDMI Rx and DisplayPort Rx is supported in GSV5800 for audio processing.

As Serdes extender, internal video codec can be enabled to support up to 4K60Hz 444 format transferred via Fiber/Coax/STP cable. Besides the video and audio transferring through Fiber/Coax/STP cable using Serdes, simultaneous dual direction Infrared, RS232 can also be supported by Gscoolink patented technology. When using Coax/STP cable, POE can also be enabled to provide power to the opposite end. GSV5800 can support up to 10Gbps for fiber module and up to 6Gbps for Coax/STP cable.

Within 4kV HBM tolerance, GSV5800's operation temperature range is -40 ºC to 85 ºC using automotive qualified process.

An internal Video Generator can be used to generate any uncompressed video timing defined in DisplayPort HBR3 bandwidth, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

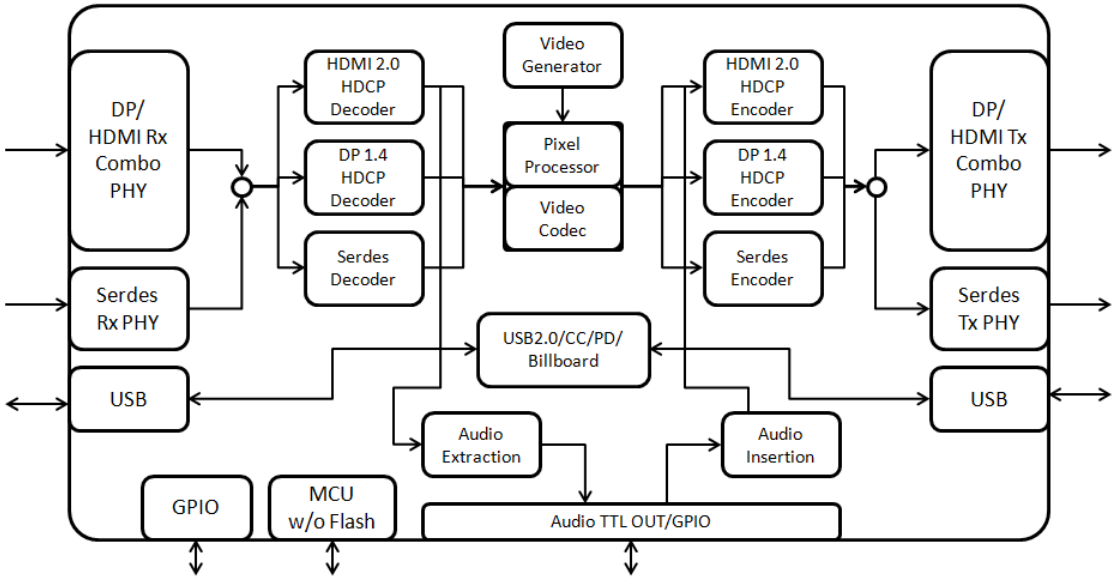



Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

| Packet ID | Packet Type | Sampling Frequency (KHz) | | |
|---|---|---|---|---|
| | | 32/44.1/48/88.2/ 96/176.4/192 | 256/352.8/384/ 512/705.6/768 | 64/128 |
| 0x02 | Audio Sample Packet (LPCM and Compressed Audio) | Y | | Y |
| 0x07 | One Bit Audio Sample Packet | Y | | |
| 0x08 | DST Audio Packet | Y | | |
| 0x09 | High Bit-rate Audio Stream Packet | Y | Y | |

# 1.2 Features

## 1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction

- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

### 1.2.2 HDMI Receiver

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- Hardware CEC Engine for Low Level protocol decoding
- 3D format support of frame packing, side-by-side, top-and-bottom

### 1.2.3 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Horizontal Blanking Reduction up to 4K@60Hz format
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

### 1.2.4 HDMI Transmitter Features

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis

- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

### 1.2.5 Serdes Transceiver

- Support 10Gbps using Fiber Extension
- Support 6Gbps using Coax/STP Extension in maximum 8 meters
- Programmable output swing , slew-rate and pre-emphasis
- Support Video/Audio Transmission
- Support up to 6 channel dual-direction Infrared/UART/GPIO transmission
- Support up to 200K baud rate for Infrared/UART/GPIO transmission

### 1.2.6 USB Type-C DisplayPort Alternative Mode Receiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Support Billboard in USB 2.0

### 1.2.7 Pixel Processor and Video Codec

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing
- Compression/Decompression of ratio 2/3/4 to lower video stream bandwidth

### 1.2.8 Audio Output and Input

- TDM8/I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx /Type-C Rx
- TDM8/I2S and SPDIF Audio Insertion to HDMI Tx/ DisplayPort Tx /Type-C Tx
- SPDIF/I2S/HBR/DSD/TDM8 Format Supported for Audio Extraction

### 1.2.9 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

# 1.3 Chip Application Modes

## 1.3.1 Type-C Alt-Mode/DisplayPort/HDMI to Serdes Conversion

RxPort could be configured as Type-C Alt-Mode (DisplayPort) Rx Input. Together with on-chip CC, USB 2.0 IP support, Type-C USB input can be configured to DisplayPort 1.4a input stream for processing. This mode is designed for transmission end of Type-C Serdes extension. RxPort could also be configured as HDMI 2.0 Input. This mode is designed for transmission end of HDMI Serdes extension.

Using uniform Serdes protocol, regardless of RxPort protocol type of Type-C Alt-Mode/DisplayPort or HDMI Input, TxPort can be configured as Type-C Alt-Mode/DisplayPort or HDMI Output.

When Serdes output is used, Type-C Alt-Mode/DisplayPort/HDMI loop back of transmission end is disabled. Internal Video Codec and Pixel Processor's Color Space Converter, De-Interlacer cannot be used at the same time.

Meanwhile, Audio extraction can be applicable if required.

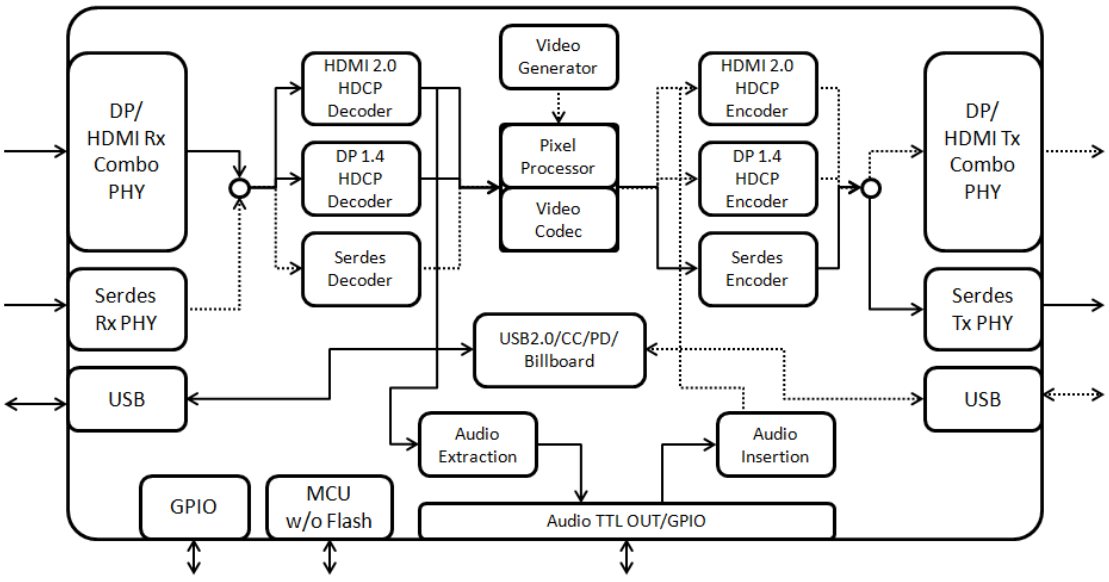



Figure 2. Type-C Alt-Mode/DisplayPort/HDMI to Serdes Application

## 1.3.2 Serdes to Type-C Alt-Mode/DisplayPort/HDMI Conversion

TxPort could be configured as Type-C Alt-Mode (DisplayPort) Tx Output. Together with on-chip CC, USB 2.0 IP support, Type-C USB output can be configured to DisplayPort

1.4a output stream for processing. This mode is designed for reception end of Type-C Serdes extension. TxPort could also be configured as HDMI 2.0 Output. This mode is designed for reception end of HDMI Serdes extension.

When Serdes input is used, Type-C Alt-Mode/DisplayPort/HDMI input are disabled. Internal Video Codec and Pixel Processor's Color Space Converter, De-Interlacer cannot be used at the same time. Cascading of GSV5800 is not supported.

Meanwhile, Audio extraction can be applicable if required.

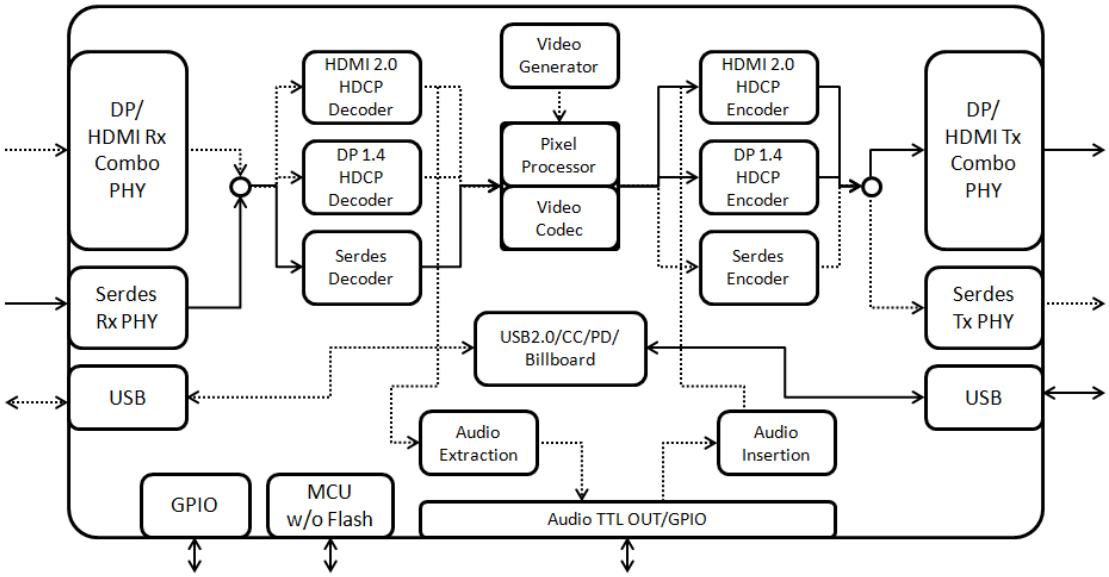



Figure 3. Serdes to Type-C Alt-Mode/DisplayPort/HDMI Application

## 1.3.3 Serdes Transparent Pass-through pin allocation

There are total 6 forward direction and 6 reverse direction transparent pass-through pins for application use. By default, all the transparent pass-through pins are push-pull configurable input/output. If required, all the transparent pass-through pins can also be configured as open-drain mode.

All AUD1/AUD2 pins are customizable for transparent pass-through use. Commonly used cases include UART/GPIO/PWM/Infrared. Each pin can support up to maximum 250Kbps.

A typical transparent pass-through application pin allocation is provided below.

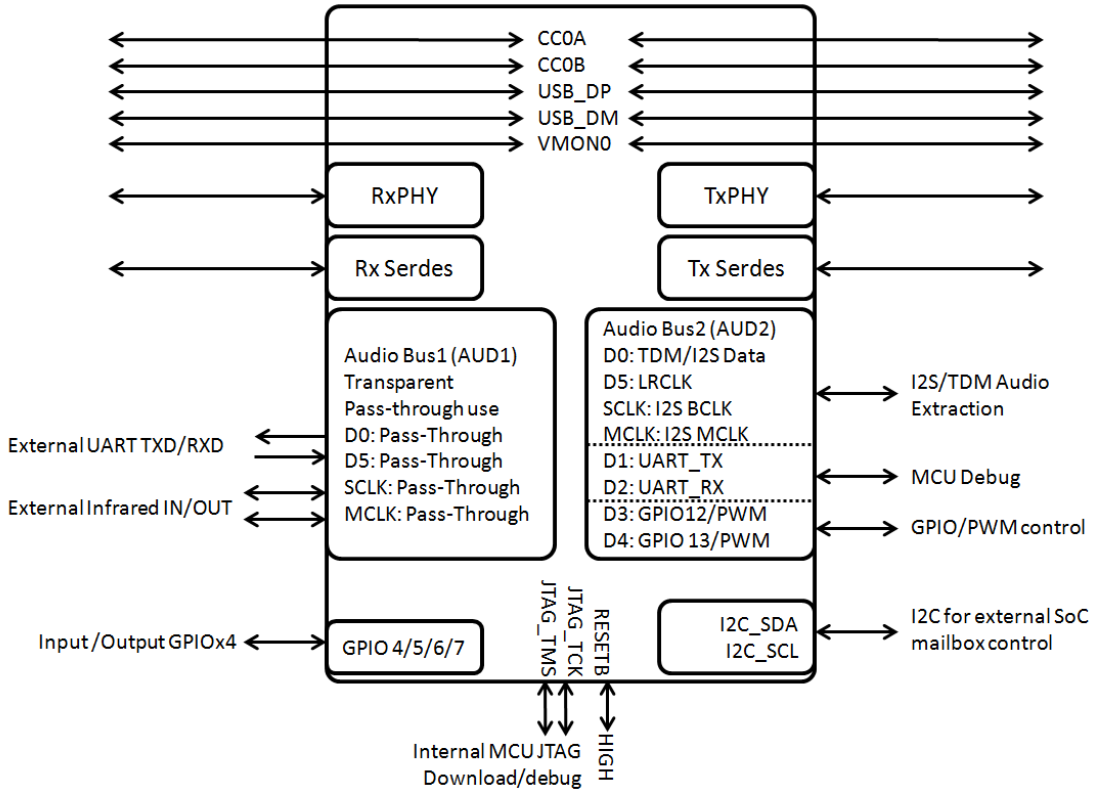



Figure 4. Typical Transparent Pass-through Pin Allocation

## 1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF needs to be muxed as output. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AUD_D0 | SDATA[0] | Output | I2S Data, default stereo channels<br>SPDIF Data when output is SPDIF |
| AUD_D5 | LRCLK/WS | Output | Fs (0 = Left, 1 = Right) using I2S |
| SCLK | BCLK | Output | Fixed to 64Fs using I2S |
| MCLK | Sys Clock | Output | Selected from 128Fs/256Fs/384Fs/512Fs using I2S |

For TDM format, a fixed format of TDM-8 can be enabled. The Format is listed as below.

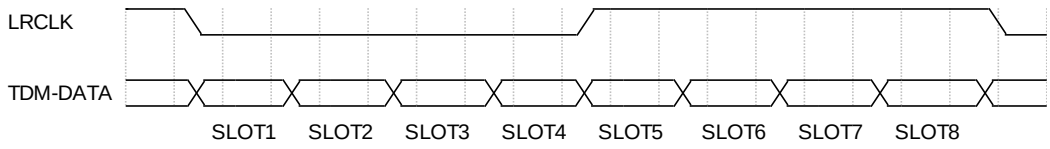



Figure 5. TDM-8 Format

Table 3. TDM Audio Extraction Format

| Slot Name | LPCM 2.0 Audio | LPCM 5.1 Audio | LPCM 7.1 Audio |
|---|---|---|---|
| SLOT1 | Stereo L | 5.1-L | 7.1-L |
| SLOT2 | Stereo R | 5.1-R | 7.1-R |
| SLOT3 | | 5.1-C | 7.1-C |
| SLOT4 | | 5.1-LFE | 7.1-LFE |
| SLOT5 | | 5.1-LS | 7.1-LS |
| SLOT6 | | 5.1-RS | 7.1-RS |
| SLOT7 | | | 7.1-LRS |
| SLOT8 | | | 7.1-RRS |

## 1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode. For SPDIF input, GSV5800 can detect Sampling Frequency and automatically update it in Channel Status in GSV software. For I2S input, software designer needs to indicate the input sampling frequency in GSV software.

Table 4. Stereo I2S Input

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AUD_D0 | SDATA[0] | Input | I2S Data, default stereo channels |
| AUD_D5 | LRCLK/WS | Input | Fs (0 = Left, 1 = Right) |
| SCLK | BCLK | Input | Fixed to 64Fs |
| MCLK | Sys Clock | Input | Selected from 128Fs/256Fs/384Fs/512Fs |

Table 5. SPDIF Input

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AUD_D0 | SPDIF | Input | SPDIF channel |

# 2. Pin Description

## 2.1 Pin Diagram

QFN76 Pin definition is defined as below.

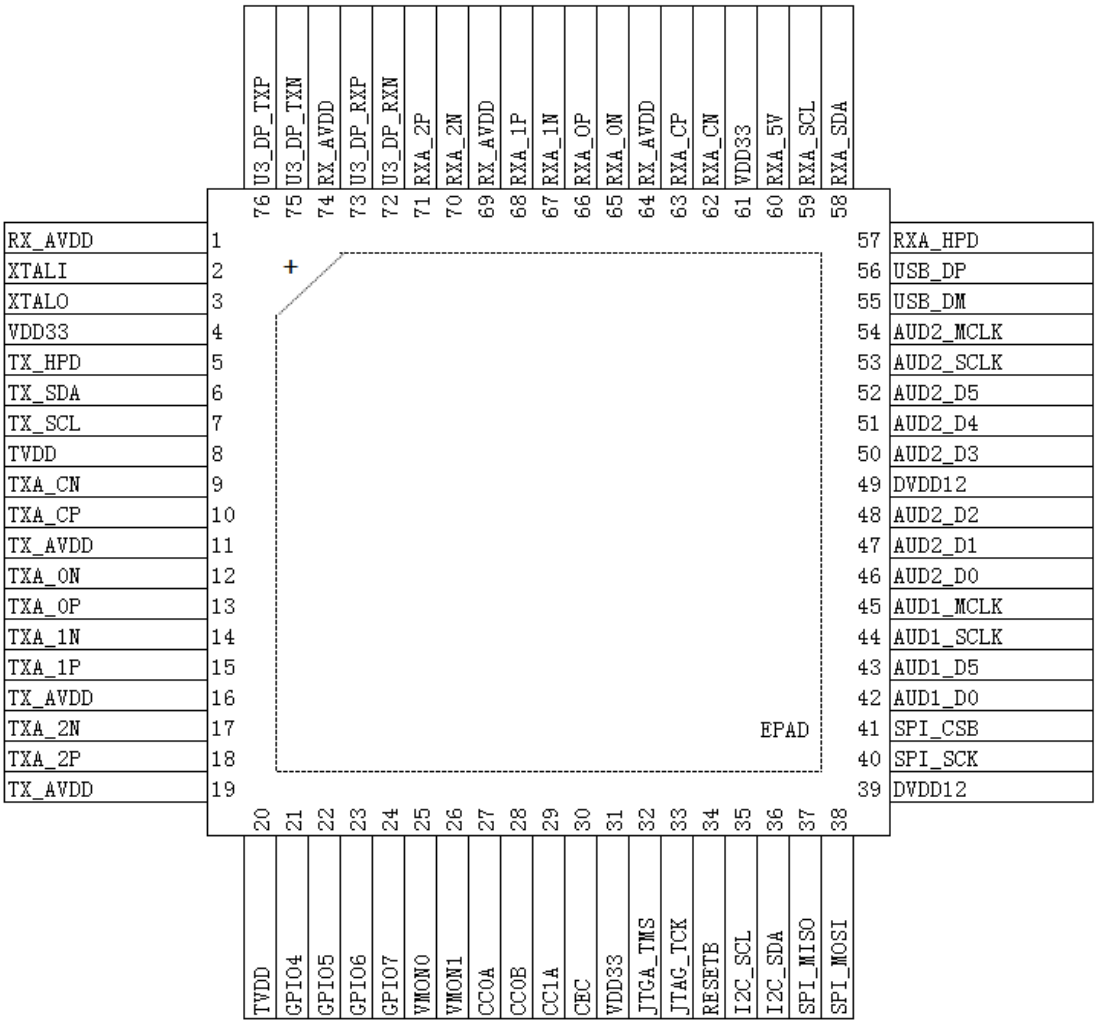



Figure 6. GSV5800 QFN76 Pin Diagram

## 2.2 QFN76 Pin Description

Table 6. QFN76 Pin Description

| Pin Name | Direction | Pin No. | Description |
|---|---|---|---|
| HDMI RX Pins/Type-C UFP/DisplayPort RX Pins | | | |
| RXA_5V | I | 60 | HDMI: RX 5V Detection PAD<br>DP: RX DP Detection PAD |
| RXA_HPD | O | 57 | HDMI: RX HPD PAD<br>DP: RX HPD PAD |

| | | | |
|---|---|---|---|
| RXA_SDA | I/O | 58 | HDMI: RX DDC SDA PAD<br>DP: RX AUX_P PAD |
| RXA_SCL | I/O | 59 | HDMI: RX DDC SCL PAD<br>DP: RX AUX_N PAD |
| RXA_CN | I | 62 | HDMI: RX Negative TMDS clock differential input<br>DP: RX Negative Main-Link differential data input [0] |
| RXA_CP | I | 63 | HDMI: RX Positive TMDS clock differential input<br>DP: RX Positive Main-Link differential data input [0] |
| RXA_0N | I | 65 | HDMI: RX Negative TMDS differential data input [0]<br>DP: RX Negative Main-Link differential data input [1] |
| RXA_0P | I | 66 | HDMI: RX Positive TMDS differential data input [0]<br>DP: RX Positive Main-Link differential data input [1] |
| RXA_1N | I | 67 | HDMI: RX Negative TMDS differential data input [1]<br>DP: RX Negative Main-Link differential data input [2] |
| RXA_1P | I | 68 | HDMI: RX Positive TMDS differential data input [1]<br>DP: RX Positive Main-Link differential data input [2] |
| RXA_2N | I | 70 | HDMI: RX Negative TMDS differential data input [2]<br>DP: RX Negative Main-Link differential data input [3] |
| RXA_2P | I | 71 | HDMI: RX Positive TMDS differential data input [2]<br>DP: RX Positive Main-Link differential data input [3] |
| Serdes Pins | | | |
| U3_DP_RXN | I/O | 72 | Serdes: RX Negative input |
| U3_DP_RXP | I/O | 73 | Serdes: RX Positive input |
| U3_DP_TXN | I/O | 75 | Serdes: TX Negative output |
| U3_DP_TXP | I/O | 76 | Serdes: TX Positive output |
| HDMI TX Pins/ Type-C DFP/DisplayPort TX Pins | | | |
| TXA_SDA | I/O | 6 | HDMI: TXA DDC SDA PAD<br>DP: TXA AUX_P PAD |
| TXA_SCL | O | 7 | HDMI: TXA DDC SCL PAD<br>DP: TXA AUX_N PAD |
| TXA_HPD | I | 5 | HDMI: TXA HPD PAD<br>DP: TXA HPD PAD |
| TXA_CN | O | 9 | HDMI: TXA Negative TMDS clock differential output<br>DP: TXA Negative Main-Link differential data output [3] |
| TXA_CP | O | 10 | HDMI: TXA Positive TMDS clock differential output<br>DP: TXA Positive Main-Link differential data output [3] |

| | | | |
|---|---|---|---|
| TXA_0N | O | 12 | HDMI: TXA Negative TMDS differential data output [0]<br>DP: TXA Negative Main-Link differential data output [2] |
| TXA_0P | O | 13 | HDMI: TXA Positive TMDS differential data output [0]<br>DP: TXA Positive Main-Link differential data output [2] |
| TXA_1N | O | 14 | HDMI: TXA Negative TMDS differential data output [1]<br>DP: TXA Negative Main-Link differential data output [1] |
| TXA_1P | O | 15 | HDMI: TXA Positive TMDS differential data output [1]<br>DP: TXA Positive Main-Link differential data output [1] |
| TXA_2N | O | 17 | HDMI: TXA Negative TMDS differential data output [2]<br>DP: TXA Negative Main-Link differential data output [0] |
| TXA_2P | O | 18 | HDMI: TXA Positive TMDS differential data output [2]<br>DP: TXA Positive Main-Link differential data output [0] |
| Power/Ground Pins | | | |
| DVDD12 | Power | 39,49, | Digital 1.2V voltage power supply |
| VDD33 | Power | 4,31,61 | Analog/Digital 3.3V voltage power supply |
| TVDD | Power | 8,20 | Analog 3.3V voltage power supply for TX Port |
| RX_AVDD | Power | 1,64,69,<br>74, | Analog 1.2V voltage power supply for RX Port |
| TX_AVDD | Power | 11,16,<br>19 | Analog 1.2V voltage power supply for TX Port |
| Digital pins | | | |
| I2C_SDA | I/O | 36 | Default: Digital IO for I2C Data<br>Alternate: GPIO8 for internal MCU |
| I2C_SCL | I/O | 35 | Default: Digital IO for I2C Clock<br>Alternate: GPIO9 for internal MCU |
| AUD1_SCLK | I/O | 44 | Digital IO PAD<br>Default: SCLK of Audio Bus 1<br>Alternate 1: GPIO3 for internal MCU control<br>Alternate 2: ADV_TIM2 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD1_MCLK | I/O | 45 | Digital IO PAD<br>Default: MCLK of Audio Bus 1<br>Alternate 1: GPIO2 for internal MCU control<br>Alternate 2: ADV_TIM1 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |

| | | | |
|---|---|---|---|
| AUD1_D0 | I/O | 42 | Digital IO PAD<br>Default: Data0 of Audio Bus 1<br>Alternate 1: GPIO0 for internal MCU control<br>Alternate 2: UART_TX for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD1_D5 | I/O | 43 | Digital IO PAD<br>Default: Data5 of Audio Bus 1<br>Alternate 1: GPIO1 for internal MCU control<br>Alternate 2: UART_RX for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_SCLK | I/O | 53 | Digital IO PAD<br>Default: SCLK of Audio Bus 2<br>Alternate 1: GPIO5 for internal MCU control<br>Alternate 2: ADV_TIM2 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_MCLK | I/O | 54 | Digital IO PAD<br>Default: MCLK of Audio Bus 2<br>Alternate 1: GPIO4 for internal MCU control<br>Alternate 2: ADV_TIM1 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_D0 | I/O | 46 | Digital IO PAD<br>Default: Data0 of Audio Bus 2<br>Alternate 1: GPIO7 for internal MCU control<br>Alternate 2: UART_TX for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_D1 | I/O | 47 | Digital IO PAD<br>Default: Data1of Audio Bus 2<br>Alternate 1: GPIO10 for internal MCU control<br>Alternate 2: UART_TX for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_D2 | I/O | 48 | Digital IO PAD<br>Default: Data2 of Audio Bus 2<br>Alternate 1: GPIO11 for internal MCU control<br>Alternate 2: UART_RX for internal MCU control<br>Alternate 3: Transparent pass-through input/output |

| | | | |
|---|---|---|---|
| AUD2_D3 | I/O | 50 | Digital IO PAD<br>Default: Data3 of Audio Bus 2<br>Alternate 1: GPIO12 for internal MCU control<br>Alternate 2: Advanced Timer1 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_D4 | I/O | 51 | Digital IO PAD<br>Default: Data4 of Audio Bus 2<br>Alternate 1: GPIO13 for internal MCU control<br>Alternate 2: Advanced Timer2 for internal MCU control<br>Alternate 3: Transparent pass-through input/output |
| AUD2_D5 | I/O | 52 | Digital IO PAD<br>Default: Data5 of Audio Bus 2<br>Alternate 1: GPIO6 for internal MCU control<br>Alternate 2: UART_RX for internal MCU control<br>Alternate 3: CEC<br>Alternate 4: Transparent pass-through input/output |
| GPIO4 | I/O | 21 | Digital IO PAD<br>GPIO4 for internal MCU control |
| GPIO5 | I/O | 22 | Digital IO PAD<br>GPIO5 for internal MCU control |
| GPIO6 | I/O | 23 | Digital IO PAD<br>GPIO6 for internal MCU control |
| GPIO7 | I/O | 24 | Digital IO PAD<br>GPIO7 for internal MCU control |
| RESETB | I | 34 | Reset Pin. Low for reset state, High for functional state. |
| XTALI | I/O | 2 | 25M Crystal Input |
| XTALO | I/O | 3 | 25M Crystal output |
| JTAG_TMS | I/O | 32 | TMS, Internal MCU programming pin |
| JTAG_TCK | I | 33 | TCK, Internal MCU programming pin |
| SPI_SCK | I/O | 40 | QSPI_SCK for QSPI Flash connection |
| SPI_CSB | I/O | 41 | QSPI_CSB for QSPI Flash connection |
| SPI_MISO | I/O | 37 | QSPI_MISO for QSPI Flash connection |
| SPI_MOSI | I/O | 38 | QSPI_MOSI for QSPI Flash connection |
| VMON0 | I/O | 25 | VBus0 Monitor Pin |
| VMON1 | I/O | 26 | VBus1 Monitor Pin |
| CC0A | I/O | 27 | Type-C CC0 Pin1 |
| CC0B | I/O | 28 | Type-C CC0 Pin2 |

| | | | |
|---|---|---|---|
| CC1A | I/O | 29 | Type-C CC1 Pin1 |
| CEC | I/O | 30 | HDMI CEC Pin, used for CEC extension<br>Require external MOS circuit to pass CEC CTS test |
| USB_DP | I/O | 56 | USB 2.0 D+ Pin |
| USB_DM | I/O | 55 | USB 2.0 D- Pin |

# 3. Electrical Specifications

## 3.1 Timing Information

### 3.1.1 Power Up and Reset Timing Diagrams

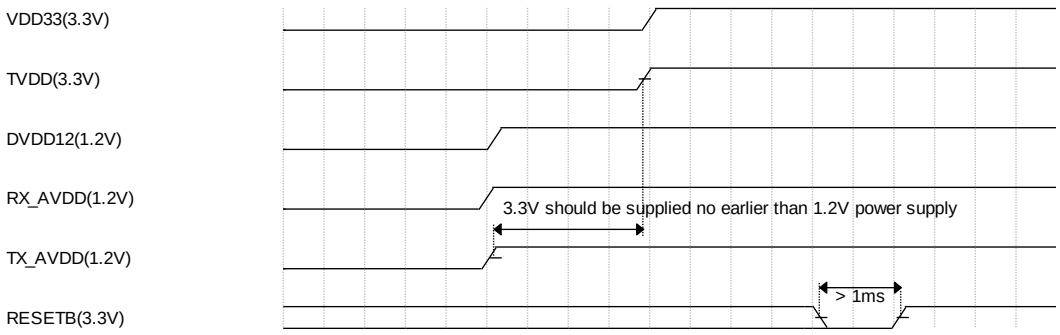



Figure 7. Power Up Sequence

## 3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

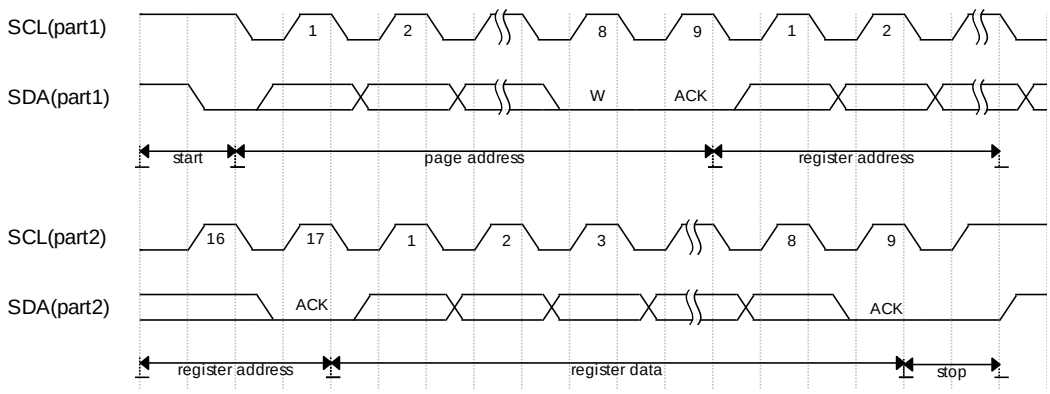



Figure 8. I2C Timing Diagram(Write)

The I2C read timing is shown below.

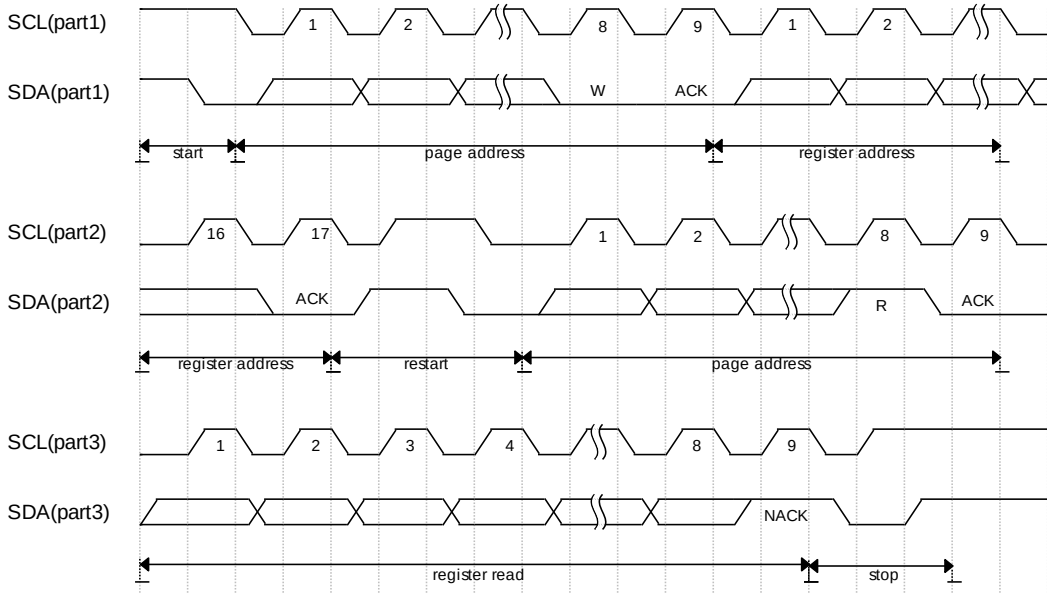



Figure 9. I2C Timing Diagram(Read)

# 3.2 Operating Conditions

## 3.2.1 Temperature Conditions

GSV5800's operation temperature range is -40 ºC to 85 ºC. The maximum junction temperature is at 125 ºC.

## 3.2.2 Audio Pin Conditions

GSV5800's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

## 3.2.3 I2C and SPI Conditions

GSV5800's I2C maximum SCL frequency is 400KHz.

Table 7. Recommended SPI Timing Conditions

| Symbol | Description | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| $f_C$ | Serial Clock Frequency | 12.5MHz | | 25 | MHz |
| $t_{CLH}$ | Serial Clock High Time | 18 | 20 | 40.11 | ns |
| $t_{CKL}$ | Clock low-level width for QSPI | 18 | 20 | 38.89 | ns |
| $t_{CLCH}$ | Serial Clock Rise Time | 0.2 | 0.63 | | V/ns |
| $t_{CHCL}$ | Serial Clock Fall Time | 0.2 | 0.66 | | V/ns |
| $t_{SLCH}$ | CS# Active Setup Time | 5 | 60 | | ns |
| $t_{CHSH}$ | CS# Active Hold Time | 5 | 104 | | ns |
| $t_{SHCH}$ | CS# Not Active Setup Time | 5 | | | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time | 5 | | | ns |
| $t_{SHSL}$ | CS# High Time (Read/Write) | 20 | 98 | | ns |
| $t_{CLQX}$ | Output Hold Time | 1.2 | 1.399 | | ns |
| $t_{DVCH}$ | Data In Setup Time | 2 | 17 | | ns |
| $t_{CHDX}$ | Data In Hold Time | 2 | 22 | | ns |
| $t_{HLCH}$ | HOLD# Low Setup Time (Relative To Clock) | 5 | | | ns |
| $t_{HHCH}$ | HOLD# High Setup Time (Relative To Clock) | 5 | | | ns |

| | | | | | |
|---|---|---|---|---|---|
| $t_{CHHL}$ | HOLD# High Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{CHHH}$ | HOLD# Low Hold Time (Relative To Clock) | 5 | | | ns |
| $t_{HLQZ}$ | HOLD# Low To High-Z Output | | | 6 | ns |
| $t_{HHQX}$ | HOLD# High To Low-Z Output | | | 6 | ns |
| $t_{CLQV}$ | Clock Low To Output Valid | | 4.999 | 7 | ns |

Table 8. Recommended I2C Timing Conditions

| Symbol | Description | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| $f_{scl}$ | Clock Cycle for QSPI | | 300 | 400 | KHz |
| $t_{LOW}$ | clock low period | 1.3 | 2 | | us |
| $t_{HIGH}$ | clock high period | 0.6 | 0.9 | | us |
| $t_{BUF}$ | bus free time before new start | 1.3 | | | us |
| $t_{VD:DAT}$ | data valid time | | | 0.9 | us |
| $t_{SU:STO}$ | set-up time for stop condition | 0.6 | 0.65 | | us |
| $t_{HD:DAT}$ | data in hold time | 0 | 1 | | us |
| $t_{SU:DAT}$ | data in setup time | 0.1 | 0.639 | | us |
| $t_R$ | rise time | | 260 | 300 | ns |
| $t_F$ | fall time | | 20 | 300 | ns |

## 3.2.4 Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Digital power supply | DVDD12 | -0.3 to 1.4 | V |
| Interface power supply | VDDIO | -0.3 to 4 | V |
| Analog power supply(RX_AVDD,MIPI_AVDD) | AVDD | -0.3 to 1.4 | V |
| Digital IO power supply | VDD33 | -0.3 to 4 | V |
| Operating Temperature Range | To | -40 to +85 | ℃ |
| Storage Temperature Range | Tstg | -40 to +125 | ℃ |
| Junction Temperature | Tj | +125 | ℃ |

## 3.2.5 ESD Protection

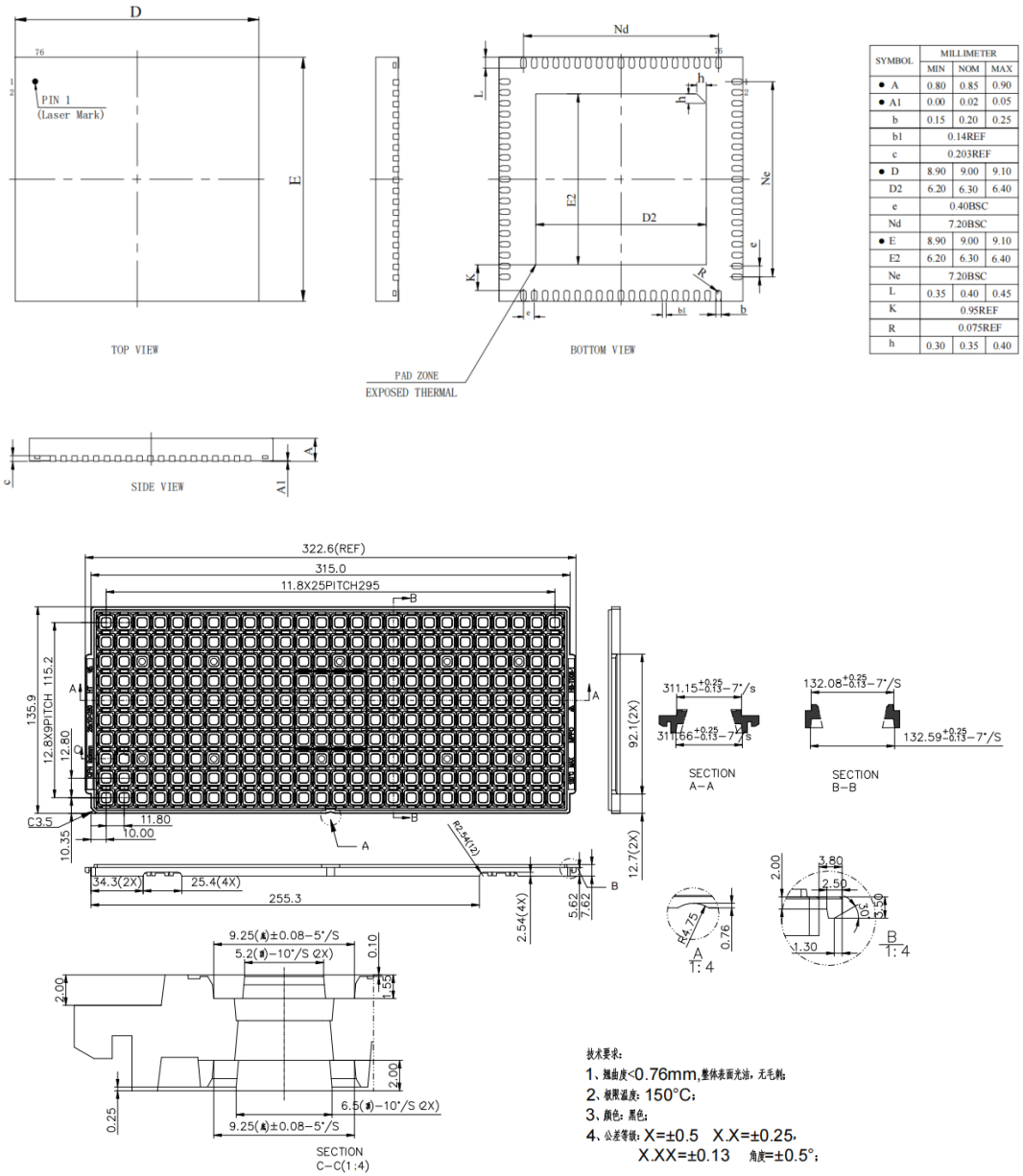
Table 10. ESD Protection

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|

| | | | |
|---|---|---|---|
| HBM | HBM for SIO(1) pins (JEDEC JS-001-2023) | 8000 | V |
| | HBM for other pins (JEDEC JS-001-2023) | 4000 | V |
| CDM | ESD CDM (JEDEC JS-002-2022) | 1000 | V |
| LU | Latch-up (JED78F) | 100 | mA |

(1) SIO : Include typeC/DP Interface and MIPI interface pins.

# 4. Package Information




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| ● A | 0.80 | 0.85 | 0.90 |
| ● A1 | 0.00 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | | 0.14REF | |
| c | | 0.203REF | |
| ● D | 8.90 | 9.00 | 9.10 |
| D2 | 6.20 | 6.30 | 6.40 |
| e | | 0.40BSC | |
| Nd | | 7.20BSC | |
| ● E | 8.90 | 9.00 | 9.10 |
| E2 | 6.20 | 6.30 | 6.40 |
| Ne | | 7.20BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | | 0.95REF | |
| R | | 0.075REF | |
| h | 0.30 | 0.35 | 0.40 |

Figure 10. Package Dimensions (QFN76)

# 5. Ordering Guide

Table 11. Ordering Information

| Part Number. | Temperature Range | Package Description | Packing Type |
|---|---|---|---|
| GSV5800 | -40°C to +85°C | QFN76 | Tray |

# 6. Revision History

Table 12. Revision history

| Revision No. | Description | Date |
|---|---|---|
| V0.1 | Draft Initial Version for internal review. | Dec 2, 2024 |
| V0.2 | Update I2C/SPI and I2S timing information | Dec 18, 2024 |
| V0.3 | Add CC1 Pin description | Dec 30, 2024 |
| V0.4 | Add TX_AVDD Pin description | Jan 13, 2025 |
| V0.5 | Fix typo of EP_* pins description | Jan 15, 2025 |
| V0.6 | Modify QFN64 to QFN76 because of AUD pin limitation | Jan 16, 2025 |
| V0.7 | Modify latch-up data | Jun 10, 2025 |
| V0.8 | Minor fix in Figures | Jul 4, 2025 |
| V0.9 | Add feature of CEC extension by modifying Pin30 from CC1B to CEC | Aug 13, 2025 |

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