# GSV9001E

Multi Purposed Video Processor

January, 2026

## Preliminary Product Specification

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# Glossary

| | |
|---|---|
| DDC | Display Data Channel |
| EDID | Extended Display Identification Data |
| HDCP | High-bandwidth Digital Content Protection |
| HDMI | High-Definition Multimedia Interface |
| HPD | Hot Plug Detect |
| UART | Universal Asynchronous Receiver Transmitter |
| $I^2C$ | Inter-Integrated Circuit |
| MCU | Microcontroller Unit |
| MISO | Master In Slave Out |
| MOSI | Master Out Slave In |
| S/PDIF | Sony/Philips Digital Interface Format |
| SPI | Serial Peripheral Interface |
| TMDS | Transition Minimized Differential Signaling |
| CEC | Consumer Electronics Control |
| AUX | AUX_CH, DisplayPort Auxiliary Channel |
| DPCD | DisplayPort Configuration Data |
| Main-Link | Unidirectional channel stream from DPTX to DPRX |
| DDC/CI | VESA Display Data Channel/Command Interface |
| MCCS | Monitor Control Command Set (VESA) |
| DP | DisplayPort (VESA) |
| DPRX | DisplayPort Receiver |
| DPTX | DisplayPort Transmitter |
| DSC | Display Stream Compression |
| FEC | Forward Error Correction |
| HBR | DisplayPort High Bit Rate, HDMI High Bit-Rate Audio |
| SSC | Spread-Spectrum Clock |
| OSD | On-screen Display |
| FRC | Frame Rate Conversion |
| PIP | Picture In Picture |
| POP | Picture Out Picture |
| HDR | High Dynamic Range |

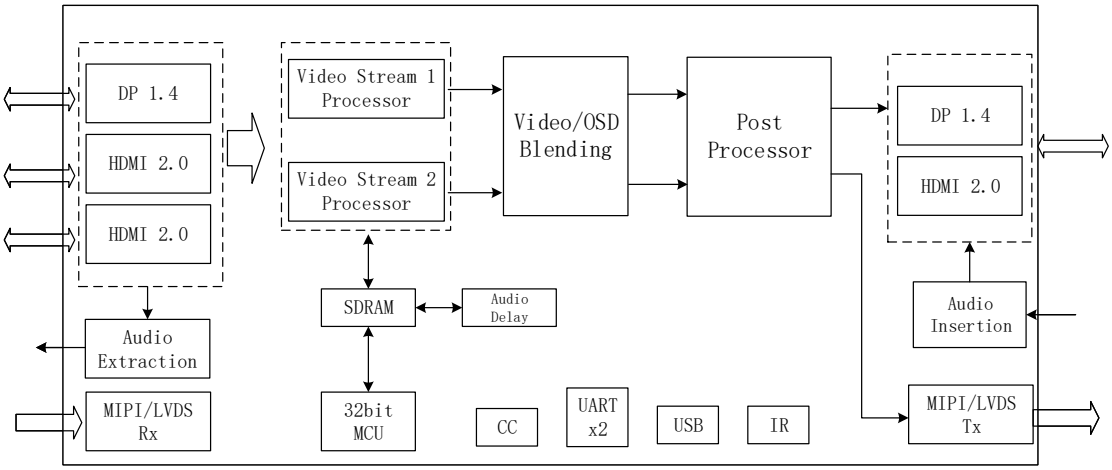
# 1 General Description

## 1.1 General Information

GSV9001E is a versatile video processor designed for a wide range of applications, including video walls, video switchers, scalers, and multi-view displays. It supports seamless switching, screen splicing, video scaling, frame rate conversion, picture quality adjustment, and OSD functions. The chip offers flexible multi-protocol support, covering HDMI 2.0/1.4, DP 1.4,eDP, MIPI CSI-2/DSI and LVDS. It also integrates low-speed bidirectional signals such as I2C and UART, making it suitable for industrial applications.

GSV9001E features arbitrary scaling and frame rate conversion capabilities. Its built-in frame buffer enables seamless switching at resolutions up to 4K 60Hz 4:4:4. Additionally, it supports frame synchronization and edge blending for comprehensive video wall implementation. The processor also provides 4-screen split view as well as PIP/PBP (Picture-in-Picture/Picture-by-Picture) display modes. Audio processing functions include audio embedding and extraction, along with automatic audio delay to maintain synchronization with the video stream.

GSV9001E incorporates a 32-bit MCU with internal flash memory, simplifying system integration and deployment.




(*) MIPI/LVDS Tx/Rx share the same PHY, which means that LVDS Tx, LVDS Rx, MIPI CSI2/DSI Tx/Rx cannot be used at the same time

Figure 1 Top Diagram

## 1.2 Features

### 1.2.1 Video Input

- 3 Channel combo PHY receiver, support HDMI2.0/DP/Serdes for each port.
- LVDS/MIPI CSI2 Receiver.
- DP Receiver：
  - Compliant with VESA DisplayPort 1.4a
  - Compliant with HDCP 2.2/2.3 and HDCP 1.4
  - Compliant with both DisplayPort and USB Type-C Alternative Mode
  - Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)

- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

■ eDP Receiver：
- Support Reduced AUX Timing
- Support ASSR

■ HDMI Receiver
- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

■ MIPI CSI2 Receiver
- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY Input
- Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

■ Dual Port LVDS Receiver
- Compatible with VESA and JEIDA standards
- Single/Dual-Port LVDS Receiver
- Data rate up to 1.5Gbps per lane

### 1.2.2 Video Output

■ Combo PHY transmitter, supports HDMI2.0/DP/eDP/Serdes

■ MIPI CSI2/DSI TX, LVDS TX

■ DP Transmitter
- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration

- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Horizontal Blanking Reduction up to 4K@60Hz format
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

■ eDP Transmitter：
- Support Reduced AUX Timing
- Support ASSR

■ HDMI Transmitter
- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), Free-Sync, G-Sync
- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

■ MIPI CSI2/DSI Transmitter
- Support MIPI CSI-2 v3.0 version transmission using D-PHY interface
- Support 2.5G bps 1/2/3/4/8-lane MIPI D-PHY Out
- Programmable output swing, slew-rate and pre-emphasis
- CSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

■ Dual-Port LVDS Transmitter
- Supports video format up to 4K60 444 10bit
- Compatible with series FPGAs' LVDS standard(12 pairs in maximum)
- Data rate up to 1.5Gbps per lane
- SDR/DDR/xN ( N =1~7) LVDS Clock transmitter with configurable output phase
- Differential VS/HS/DE available
- Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
- Single/Dual-Port LVDS Transmitter
- Support Spread Spectrum Clock (SSC)
- Programmable output swing, slew-rate, common voltage and pre-emphasis

■ TTL Transmitter
- 24-bit TTL Video Output to 1080P60 444 24bit

- Programmable drive strength, slew rate, driver disabled state control
- SDR/DDR Clock Output with configurable output phase
- Data rate up to 150Msps per lane
- HS/VS/DE available
- Embedded SAV/EAV mode supported

### 1.2.3 Video Process

- Maximum resolution: 4K60 444, up to 600MHz pixel rate
- Frame Rate Conversion (FRC)
  - Frame rate conversion from 3~250Hz to 3~250Hz
  - Arbitrary conversion ratio
- Arbitrary resolution video cropping
- Arbitrary ratio video scaling
  - Minimum Resolution 16x16, Maximum Resolution 4096x4096
  - Border fusion scaling for video wall application
- Seamless Switch
  - Input Video Source Garbage Free Seamless Switch
  - Input Video Resolution/Format Garbage Free Seamless Switch
  - Cable unplugging and plugging Garbage Free display
  - Scaling/Crop output resolution seamlessly change
- Display Functions
  - Programmable output display sizing & positioning
  - PIP or POP display
  - Programmable Alpha coefficient blending
  - Layer Freeze, Mirror & Flip
- Picture Quality
  - Automatic contrast enhancement
  - Programmable brightness, contrast, hue, saturation control
  - Programmable white balance control
- LUT Transformation
  - Gamma/logarithmic/exponential corrections for RGB/YCbCr channels
  - Piecewise linear transformation with 256 knee points
- Low output latency frame lock mode
  - Input video frame lock
  - 2ms maximum (VBlank of output timing) for output latency
  - External sync source frame lock
  - Programmable vertical delay
- Video Rotation
  - Single Layer 90/180/270 video rotation
  - Up to 1080p60 resolution
- Other
  - Edge Adaptive I2P
  - P2I

- HDR2SDR
- YUV444/420 interconversion
- YUV444/422 interconversion
- Arbitrary coefficient color space conversion
- Test pattern generator
- Startup/standby screen display

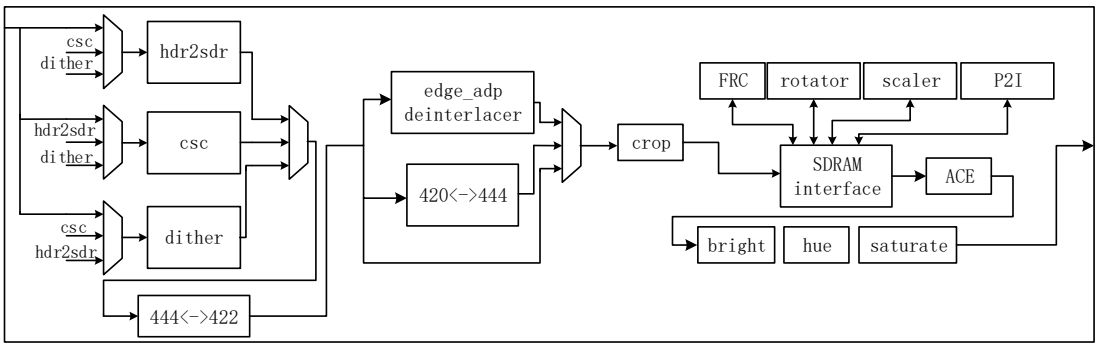



Figure 2 Video Process Flow

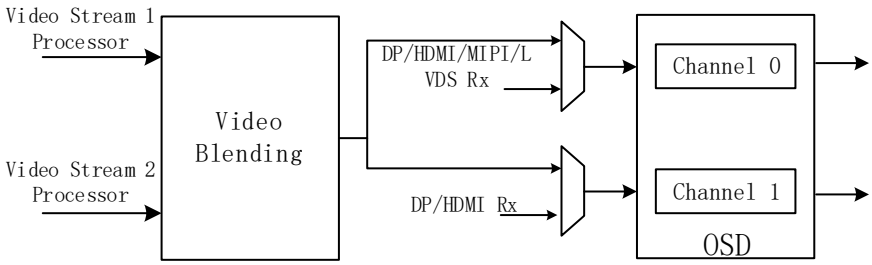



Figure 3 Video/OSD Blending Flow

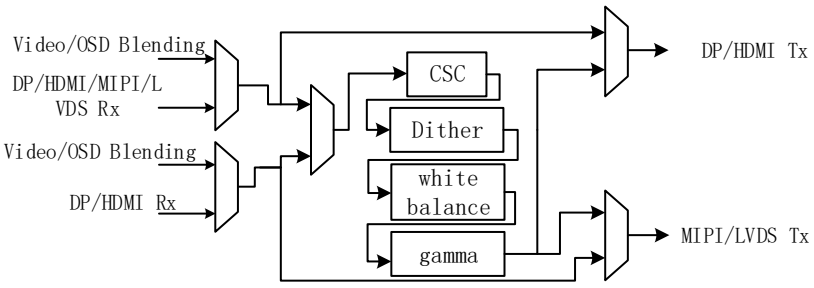



Figure 4 Post Process Flow

### 1.2.4 OSD

- Dual channel OSD, for DP/HDMI/Serdes Tx, of MIPI/LVDS Tx, able to output different timing at the same time
- Support overall color adjustment and position adjustment of graphics
- Support graphics scaling
- Support frame operation
- 64 layers in total, 128 levels of alpha effect
- Up to 128 rectangular regions, for edges of each regions are displayed independently
- Support rounded corners

- Support region background gradient color
- Up to 256 characters in a single region
- Horizontal and vertical layout for characters
- Independent parameter configuration for each character
- The storage format of characters and icons is consistent
- Up to 256x256 pixels for a single character
- 1/2/4/8/16/32 bit modes for character pixel
- 256 color index character color
- Support non-monospaced fonts

### 1.2.5 Other

- Bi-directional transmission
- Embedded MCU
  - 32-bit RISCV core with 100MHz operation
  - Internal SRAM: 12KB instruction memory and 16KB data memory
  - JTAG debugger mode
- Peripheral Interface
  - I2C: Master and Slave
  - SPI: Master and Slave
  - 2 UARTs
  - Timer and PWM
  - Watchdog Timer
  - Interrupt controller
  - GPIO
  - ADC
- Audio
  - I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx /Type-C Rx
  - I2S and SPDIF Audio Insertion to HDMI Tx/ DisplayPort Tx /Type-C Tx
  - SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction
  - Programable audio delay timing for audio and video synchronization

## 1.3 Chip Application Modes

### 1.3.1 Videowall

GSV9001E can be configured as spliced screen embedded display processor. There are two implementation options available, cascade and parallel.

As shown in Figure 4, in cascade mode, GSV9001E transmits received video directly to downstream board, and processes the video for panel display. Control information can be transmitted on the same cable through the bidirectional transmission function of GSV9001E.

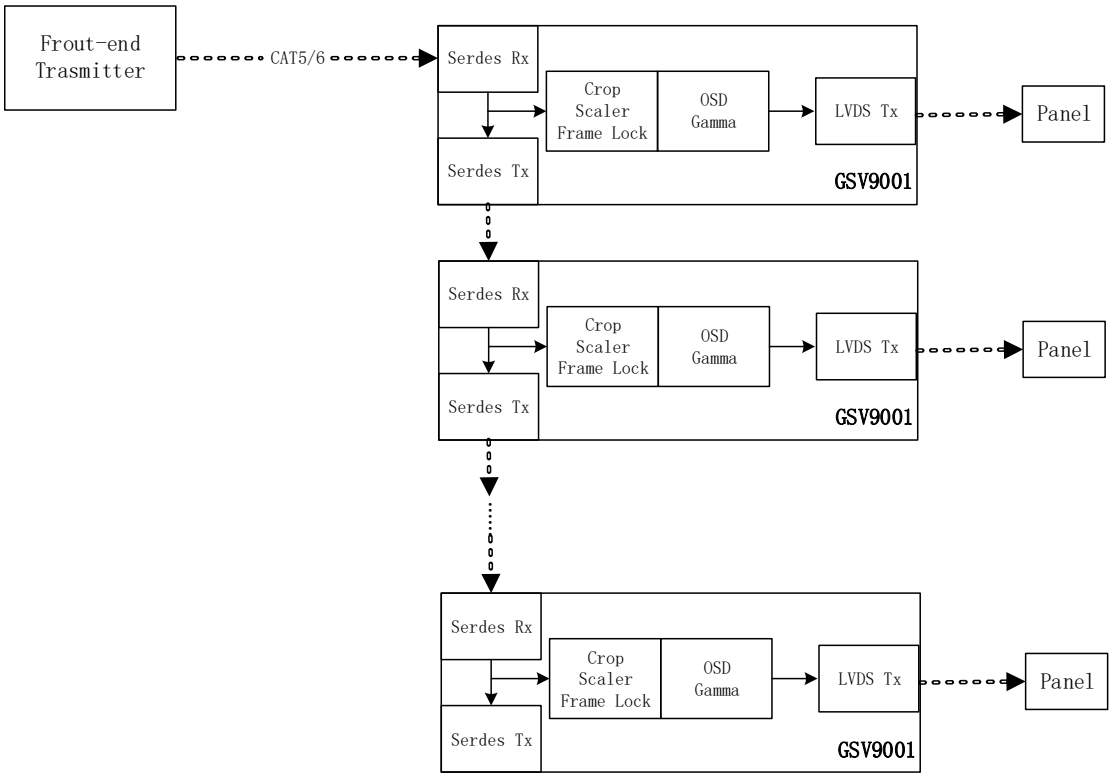



Figure 5 Cascade Mode Videowall

As shown in Figure 5, GSV9001E can also be deployed in parallel splicing solutions.

In both solutions, strict synchronization between multiple panels can be achieved by frame lock. The synchronization source can be either the input video or an external sync pulse. The displayed delay can be configured in lines.

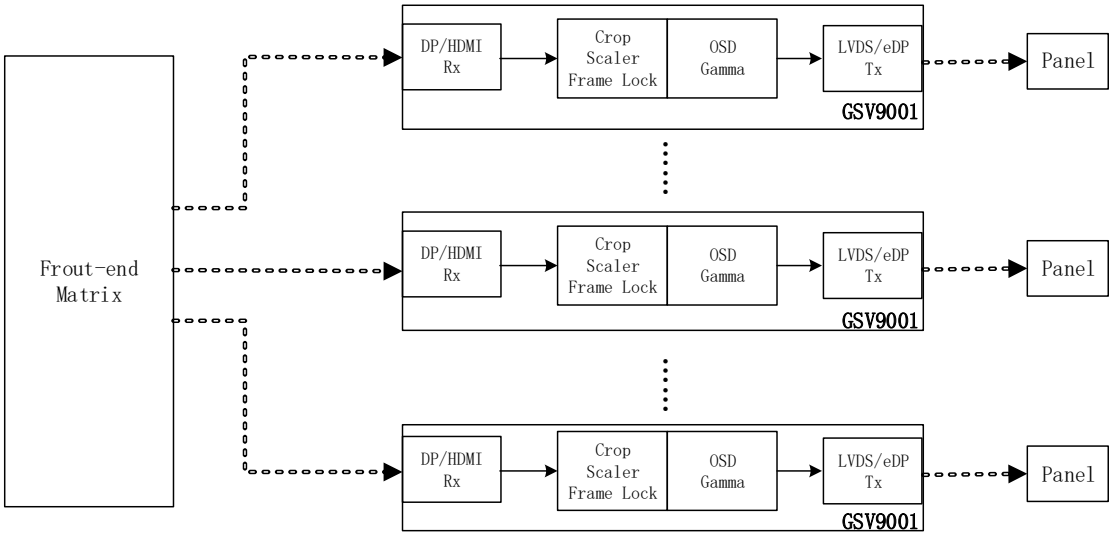



Figure 6 Parallel Mode Videowall

### 1.3.2 Seamless Switch

GSV9001E is able to process video up to 4k60 444, with DP 2lane 8.1G. Therefore, GSV9001E can

be used with a SERDES switch to achieve display screen switching without junk frames or black screens through its own stable detection of input signals and frame buffer structure.

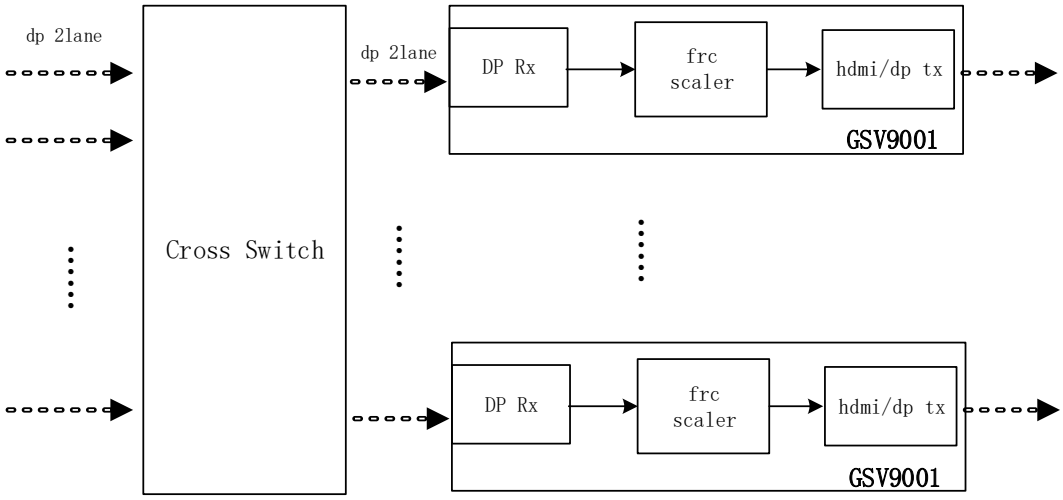
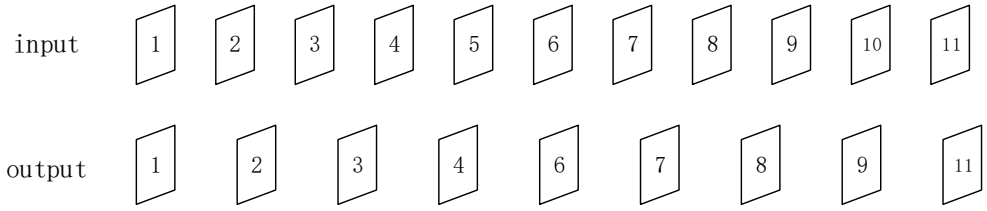
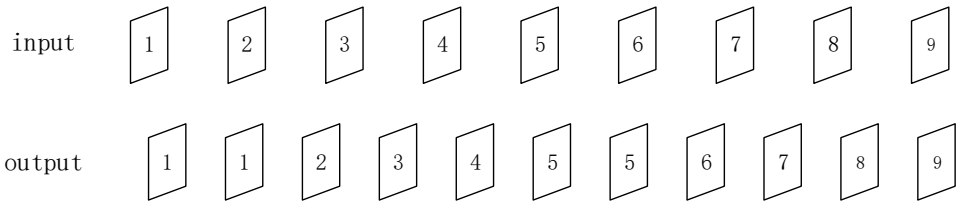



Figure 7 Seamless Switch Schematic

To achieve this effect, clock and timing of Tx runs in free-run mode or external sync mode. In this mode, the output and input video are not synchronized, and FRC must be required. That is, any input timing is converted to free-run timing. GSV9001E achieves up-conversion and down-conversion by repeatedly reading the frame buffer and discarding the frame buffer.




(a) Down-conversion FRC




(b) Up-conversion FRC

Figure 8 FRC implementing

GSV9001E can scale while implementing FRC, the input video can be switched to any resolution between 4096x4096 to 16x16.

In addition, the GSV9001E can be used as a seamless switcher alone.

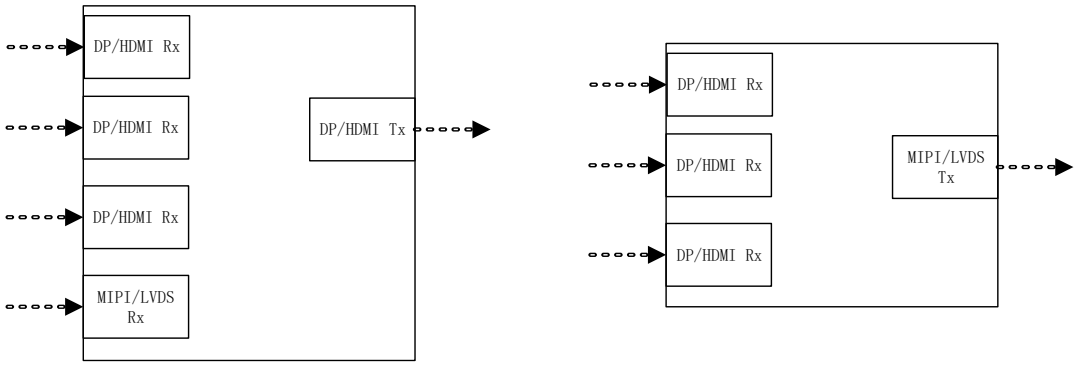



Figure 9 Seamless Switcher Application Mode

### 1.3.3 Scaler Controller

GSV9001E supports to be configured as scaler controller. Up to 3 channels input, with 2 channel process and blending.

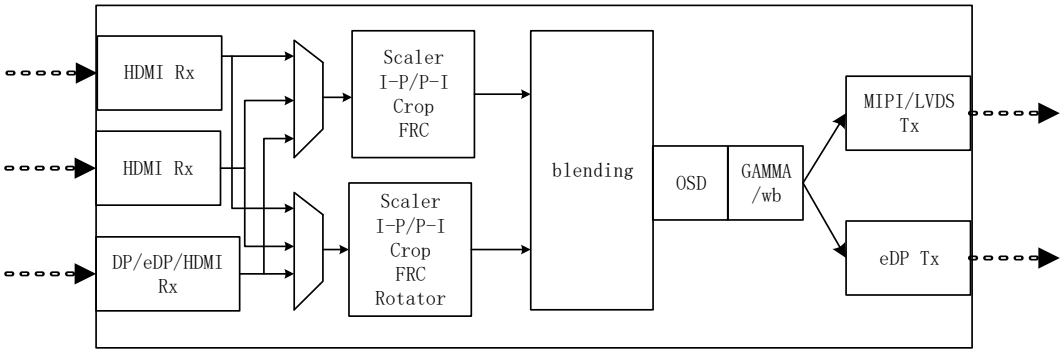



Figure 10 Scaler Controller Schematic

In this mode, two of the three-channel inputs can be regarded as two layers after scaling, I-P, P-I, FRC, etc. These two layers can be placed or superimposed in any position relationship. The position, size, and transparency of the layer are all switched seamlessly.

Up to 600MHz pixel rate, or 4K60/1080P120 resolution is supported.

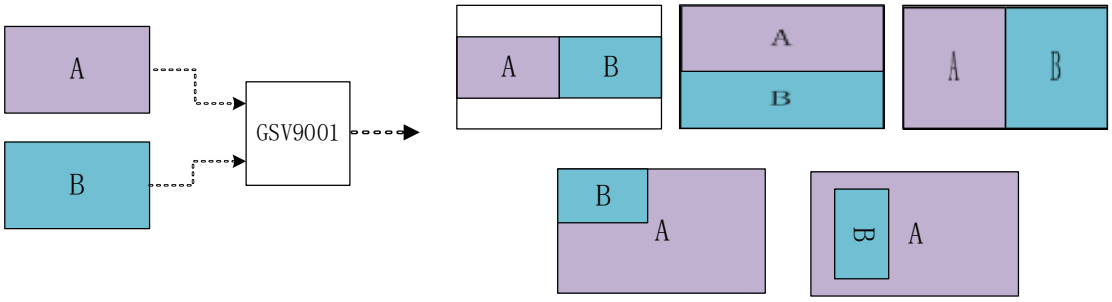



Figure 11 Double Channel Video Process

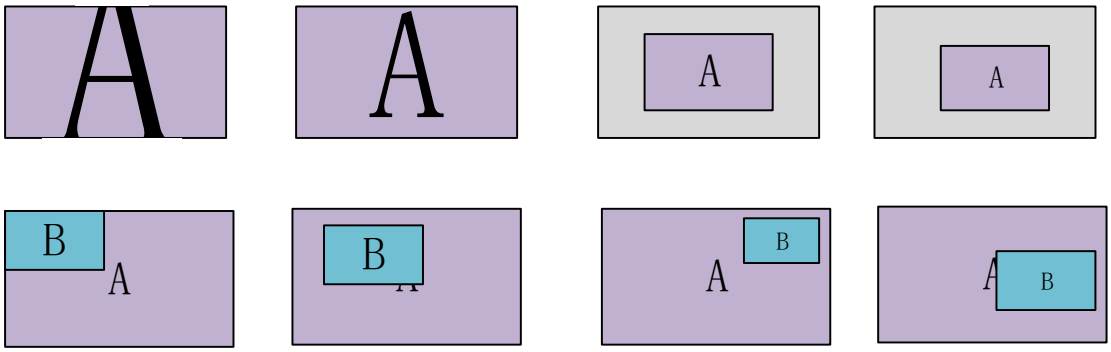



Figure 12 Seamless Position and Size Change

### 1.3.4 Multi-view Display

When two GSV9001E are implemented, a quad-view display can be achieved. In such an implementation, video streaming A and B are superimposed into the same streaming in chip A and output to chip B. The connection between A & B supposed to be 2 lane DP, which can transmit up to 4K60 resolution. The superimposed image is used as the background in chip B and superimposed with C and D to achieve a multi view effect. It should be noted that the four screens can have any positional relationship, but if the screens need to be superimposed, screen A and screen B can only be at the lower level, that is, screen A and screen B will always be covered by screen C and screen D. Likewise, using more GSV9001E can achieve more images.

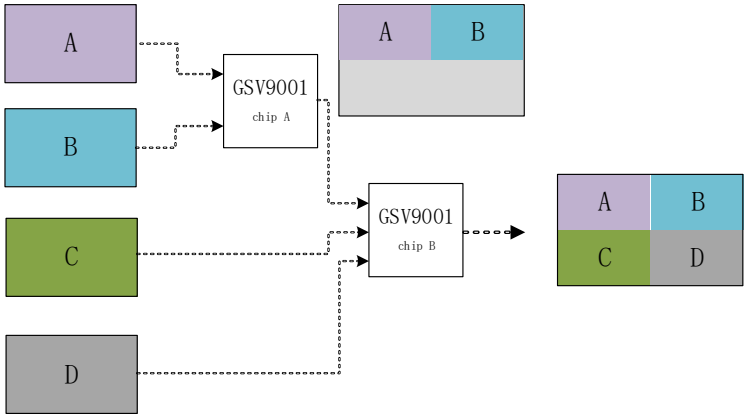



Figure 13 4 Inputs Multiview

### 1.3.5 OSD

OSD can be implemented with all the above applications. OSD can be used on both outputs. OSD can work on two outputs. One of them can be from the video after FRC, scaling, crop, rotation, blending, etc., and the other can be any video input. Or both can come from the video input.

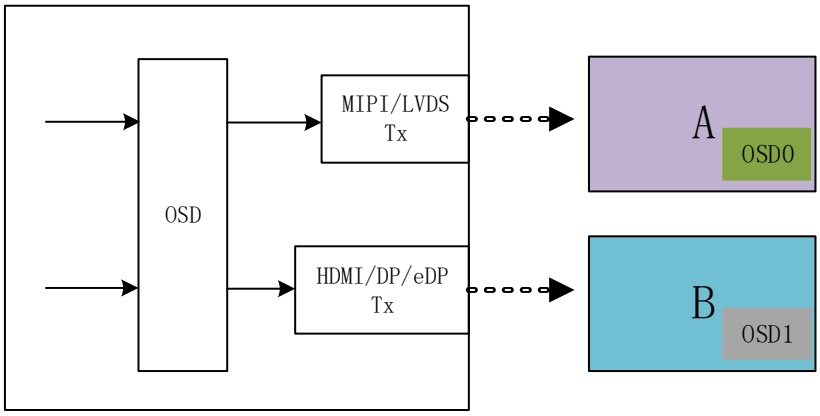



Figure 14 Double Channel OSD Application

An independent coordinate system that supports negative coordinates is implemented in OSD, which is used to set the position of OSD region and OSD show-area. Region/show-area can be set arbitrarily in the coordinate system. Only regions that intersect with show-area will be composed into OSD video. OSD video can be scaled/color adjusted/CSC before being superimposed with input video. The superimposed coordinates (relative to input video) can be set.

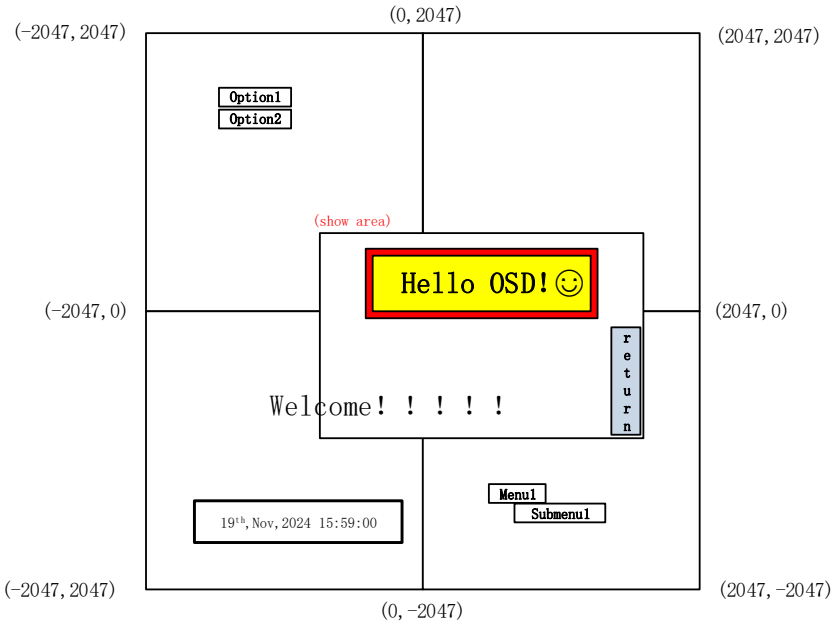



Figure 15 OSD Coordinate system

OSD contains foreground layer/region layer/background layer/input video layer, of which there are 64 region layers in total. The foreground layer/region layer is first synthesized with the OSD video and then alpha-superimposed with the background layer and the input video layer. Each region layer can contain any number of regions, and each region is divided into two layers, the border background layer and the data string layer; the border background layer is used to display the border and background of the region, and the data string layer displays the text/icon of the region.

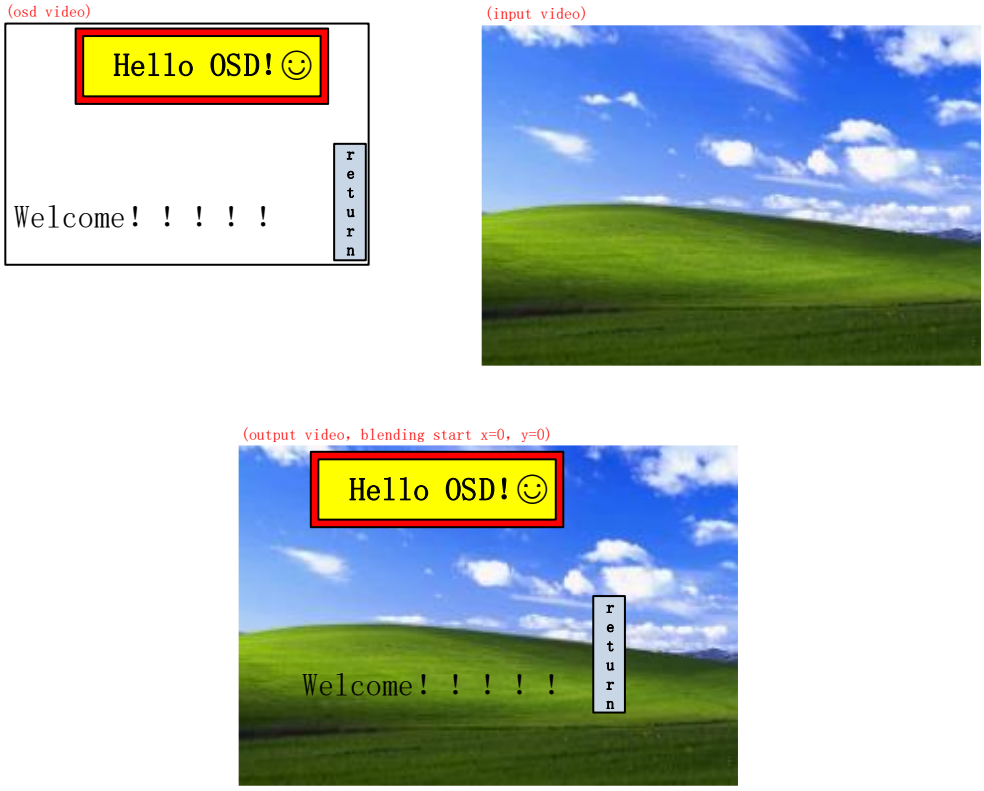



Figure 16 OSD Display Effect

# 2 Pin Description

## 2.1 Pin Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | RXC_2P | RXC_1P | RXC_0P | RXC_CP | AVDD12 | RXB_2P | RXB_1P | RXB_0P | RXB_CP | AVDD12 | RXA_2P | RXA_1P | RXA_0P | RXA_CP | GND |
| B | GND | RXC_2N | RXC_1N | RXC_0N | RXC_CN | AVDD12 | RXB_2N | RXB_1N | RXB_0N | RXB_CN | AVDD12 | RXA_2N | RXA_1N | RXA_0N | RXA_CN | GND |
| C | TXA_CP | TXA_CN | VDD33 | AVDD12 | AVDD12 | AVDD12 | VDD33 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | RXC_5V | RXC_HPD | ALSB | NC | REXT400 |
| D | TXA_0P | TXA_0N | VDD33 | XTALO | XTALI | GND | VDD33 | VDD33 | DVDD12 | DVDD12 | RXC_SDA | RXC_SCL | RXB_5V | RXB_SCL | RXB_SDA | RXB_HPD |
| E | TXA_1P | TXA_1N | TX_TVDD | TX_TVDD | AVDD12 | AVDD12 | GND | VDD33 | GND | GND | GND | GND | RXA_5V | RXA_SCL | RXA_SDA | RXA_HPD |
| F | TXA_2P | TXA_2N | AVDD12 | AVDD12 | GND | GND | GND | GND | DVDD12 | DVDD12 | GND | GND | AUD2_MCLK | AUD2_SCLK | AUD2_D5 | AUD2_D4 |
| G | GND | GND | AVDD12 | AVDD12 | GND | DVDD12 | DVDD12 | GND | GND | GND | GND | GND | AUD2_D3 | AUD2_D2 | AUD2_D1 | AUD2_D0 |
| H | DPHYA_0P | DPHYA_0N | DVDD12 | DVDD12 | GND | GND | GND | GND | GND | GND | DDR_VDDIO | DDR_VDDIO | AUD1_MCLK | AUD1_SCLK | AUD1_D5 | AUD1_D4 |
| J | DPHYA_1P | DPHYA_1N | GND | GND | GND | GND | GND | GND | DVDD12 | DVDD12 | DDR_GND | DDR_GND | AUD1_D3 | AUD1_D2 | AUD1_D1 | AUD1_D0 |
| K | DPHYA_2P | DPHYA_2N | AVDD12 | AVDD12 | GND | GND | GND | GND | GND | GND | DDR_VDDIO | DDR_VDDIO | GPIO7 | GPIO6 | GPIO5 | GPIO4 |
| L | DPHYA_3P | DPHYA_3N | VDDIO | AVDD12 | AVDD12 | VDD33 | DVDD12 | DVDD12 | GND | GND | DDR_GND | DDR_GND | I2C_SDA | I2C_SCL | GPIO9 | GPIO8 |
| M | DPHYA_4P | DPHYA_4N | VDDIO | GND | GND | GND | GND | GND | GND | GND | DDR_VDDIO | DDR_VDDIO | DDR_VREFCA | DDR_ZQ | INT | AVMUTE |
| N | DPHYA_5P | DPHYA_5N | VDDIO | VMONO | CCOB | USB_DP | TXA_HPD | TXA_SCL | JTAG2 | GND | DDR_GND | DDR_GND | DDR_VREFDQ | NC | QS_MISO | QS_MOSI |
| P | DPHY_VSP | DPHY_VSN | VDDIO | CCOA | CEC | USB_DM | TXA_SDA | TXA_UTILTY | JTAG1 | RESETB | DDR_VDDIO | DDR_VDDIO | DDR_GND | DDR_GND | QS_SCK | QS_CSB |
| R | DPHY_HSP | DPHY_HSN | DPHY_CN | DPHY_DEN | DPHYB_0N | DPHYB_1N | DPHYB_2N | DPHYB_3N | DPHYB_4N | DPHYB_5N | DDR_GND | DDR_GND | DDR_VDDIO | DDR_VDDIO | QS_WPB | QS_HOLDB |
| T | GND | GND | DPHY_CP | DPHY_DEP | DPHYB_0P | DPHYB_1P | DPHYB_2P | DPHYB_3P | DPHYB_4P | DPHYB_5P | DDR_VDDIO | DDR_VDDIO | DDR_VDDIO | DDR_GND | DDR_GND | DDR_GND |

Figure 17 Pin Diagram

## 2.2 Pin Description

| Pin Name | Direction | Pin No. | Description |
|---|---|---|---|
| HDMI RX Pins/Type-C UFP/DisplayPort RX Pins | | | |
| RXA_5V | I | E13 | HDMI: RXA 5V Detection PAD<br>DP: RXA DP Detection PAD |
| RXA_HPD | I/O | E16 | HDMI: RXA HPD PAD<br>DP: RXA HPD PAD |
| RXA_SDA | I/O | E15 | HDMI: RXA DDC SDA PAD<br>DP: RXA AUX_P PAD |
| RXA_SCL | I/O | E14 | HDMI: RXA DDC SCL PAD<br>DP: RXA AUX_N PAD |
| RXA_CN | I | B15 | HDMI: RXA Negative TMDS clock differential input<br>DP: RXA Negative Main-Link differential data input [0] |
| RXA_CP | I | A15 | HDMI: RXA Positive TMDS clock differential input<br>DP: RXA Positive Main-Link differential data input [0] |
| RXA_0N | I | B14 | HDMI: RXA Negative TMDS differential data input [0]<br>DP: RXA Negative Main-Link differential data input [1] |
| RXA_0P | I | A14 | HDMI: RXA Positive TMDS differential data input [0]<br>DP: RXA Positive Main-Link differential data input [1] |
| RXA_1N | I | B13 | HDMI: RXA Negative TMDS differential data input [1]<br>DP: RXA Negative Main-Link differential data input [2] |
| RXA_1P | I | A13 | HDMI: RXA Positive TMDS differential data input [1]<br>DP: RXA Positive Main-Link differential data input [2] |
| RXA_2N | I | B12 | HDMI: RXA Negative TMDS differential data input [2]<br>DP: RXA Negative Main-Link differential data input [3] |
| RXA_2P | I | A12 | HDMI: RXA Positive TMDS differential data input [2]<br>DP: RXA Positive Main-Link differential data input [3] |
| | | | |
| RXB_5V | I | D13 | HDMI: RXB 5V Detection PAD<br>DP: RXB DP Detection PAD |
| RXB_HPD | I/O | D16 | HDMI: RXB HPD PAD<br>DP: RXB HPD PAD |
| RXB_SDA | I/O | D15 | HDMI: RXB DDC SDA PAD<br>DP: RXB AUX_P PAD |
| RXB_SCL | I/O | D14 | HDMI: RXB DDC SCL PAD<br>DP: RXB AUX_N PAD |
| RXB_CN | I | B10 | HDMI: RXB Negative TMDS clock differential input<br>DP: RXB Negative Main-Link differential data input [0] |

| | | | |
|---|---|---|---|
| RXB_CP | I | A10 | HDMI: RXB Positive TMDS clock differential input<br>DP: RXB Positive Main-Link differential data input [0] |
| RXB_0N | I | B9 | HDMI: RXB Negative TMDS differential data input [0]<br>DP: RXB Negative Main-Link differential data input [1] |
| RXB_0P | I | A9 | HDMI: RXB Positive TMDS differential data input [0]<br>DP: RXB Positive Main-Link differential data input [1] |
| RXB_1N | I | B8 | HDMI: RXB Negative TMDS differential data input [1]<br>DP: RXB Negative Main-Link differential data input [2] |
| RXB_1P | I | A8 | HDMI: RXB Positive TMDS differential data input [1]<br>DP: RXB Positive Main-Link differential data input [2] |
| RXB_2N | I | B7 | HDMI: RXB Negative TMDS differential data input [2]<br>DP: RXB Negative Main-Link differential data input [3] |
| RXB_2P | I | A7 | HDMI: RXB Positive TMDS differential data input [2]<br>DP: RXB Positive Main-Link differential data input [3] |
| | | | |
| RXC_5V | I | C12 | HDMI: RXC 5V Detection PAD<br>DP: RXC DP Detection PAD |
| RXC_HPD | I/O | C13 | HDMI: RXC HPD PAD<br>DP: RXC HPD PAD |
| RXC_SDA | I/O | D11 | HDMI: RXC DDC SDA PAD<br>DP: RXC AUX_P PAD |
| RXC_SCL | I/O | D12 | HDMI: RXC DDC SCL PAD<br>DP: RXC AUX_N PAD |
| RXC_CN | I | B5 | HDMI: RXC Negative TMDS clock differential input<br>DP: RXC Negative Main-Link differential data input [0] |
| RXC_CP | I | A5 | HDMI: RXC Positive TMDS clock differential input<br>DP: RXC Positive Main-Link differential data input [0] |
| RXC_0N | I | B4 | HDMI: RXC Negative TMDS differential data input [0]<br>DP: RXC Negative Main-Link differential data input [1] |
| RXC_0P | I | A4 | HDMI: RXC Positive TMDS differential data input [0]<br>DP: RXC Positive Main-Link differential data input [1] |
| RXC_1N | I | B3 | HDMI: RXC Negative TMDS differential data input [1]<br>DP: RXC Negative Main-Link differential data input [2] |

| | | | |
|---|---|---|---|
| RXC_1P | I | A3 | HDMI: RXC Positive TMDS differential data input [1]<br>DP: RXC Positive Main-Link differential data input [2] |
| RXC_2N | I | B2 | HDMI: RXC Negative TMDS differential data input [2]<br>DP: RXC Negative Main-Link differential data input [3] |
| RXC_2P | I | A2 | HDMI: RXC Positive TMDS differential data input [2]<br>DP: RXC Positive Main-Link differential data input [3] |
| HDMI TX Pins/ Type-C DFP/DisplayPort TX Pins | | | |
| TXA_SDA | I/O | P7 | HDMI: TXA DDC SDA PAD<br>DP: TXA AUX_P PAD |
| TXA_SCL | O | N8 | HDMI: TXA DDC SCL PAD<br>DP: TXA AUX_N PAD |
| TXA_UTILITY | I | P8 | |
| TXA_HPD | I | N7 | HDMI: TXA HPD PAD<br>DP: TXA HPD PAD |
| TXA_CN | O | C2 | HDMI: TXA Negative TMDS differential data output [3]/ TMDS clock differential output<br>DP: TXA Negative Main-Link differential data output [3] |
| TXA_CP | O | C1 | HDMI: TXA Positive TMDS differential data output [3]/ TMDS clock differential output<br>DP: TXA Positive Main-Link differential data output [3] |
| TXA_0N | O | D2 | HDMI: TXA Negative TMDS differential data output [0]<br>DP: TXA Negative Main-Link differential data output [2] |
| TXA_0P | O | D1 | HDMI: TXA Positive TMDS differential data output [0]<br>DP: TXA Positive Main-Link differential data output [2] |
| TXA_1N | O | E2 | HDMI: TXA Negative TMDS differential data output [1]<br>DP: TXA Negative Main-Link differential data output [1] |
| TXA_1P | O | E1 | HDMI: TXA Positive TMDS differential data output [1]<br>DP: TXA Positive Main-Link differential data output [1] |
| TXA_2N | O | F2 | HDMI: TXA Negative TMDS differential data output [2]<br>DP: TXA Negative Main-Link differential data output [0] |
| TXA_2P | O | F1 | HDMI: TXA Positive TMDS differential data output [2]<br>DP: TXA Positive Main-Link differential data output [0] |
| Power/Ground Pins | | | |

| | | | |
|---|---|---|---|
| DVDD12 | Power | D9, D10, F9, F10, G6 ,G7, J9, H3, H4, L7, L8 | Digital 1.2V voltage power supply |
| VDD33 | Power | D8, E8, C7, D7, D8, E8, L6 | 3.3V voltage power supply |
| VDDIO | Power | L3,M3, N3, P3 | Voltage power supply for Parallel Port, 1.8/2.5/3.3V optional |
| AVDD12 | Power | A6, B6, A11, B11, C4, C5, C6, C8, C9, C10, C11, E5, E6, F3, F4, G3, G4, K3, K4, L4, L5 | Analog 1.2V voltage power supply |
| DVDD12 | Power | D9, D10, F9, F10, G6, G7, H3, H4, J9, J10, L7, L8 | Digital 1.2V voltage power supply |
| TX_TVDD | Power | E3, E4 | Terminal 3.3V voltage power supply for TX Port, board level diode isolation is required. |
| DDR_VDDIO | Power | H11, H12, K11, K12, M11, M12, P 11, P12, R13, R14, T11, T12, T13 | DDR3 power supply, 1.35V. |
| GND | Ground | A1, A16, B1, B16, D6, E7, E9, E10, E11, E12, F5, F6, F7, F8, F11, F12, G1, G2, G5, G8, G9, G10, G11, G12, H5, H6, H7, H8, H9, H10, J3, J4, J5, J6, J6, J7, K5, K6, K7, K8, K9, K10, L9, L10, M4, M5, M6, M7, M8, M9, M10, N10, T1, T2 | Ground |
| DDR_GND | Ground | J11, J12, L11, L12, N11, N12, P13, P14, R11, R12, T14, T15, T16 | Ground for DDR IO |
| MIPI Tx/Rx Pins | | | |
| DPHY_CP | I/O | T3 | LVDS: LVDS clock differential positive output<br>TTL: LVDS clock output |
| DPHY_CN | I/O | R3 | LVDS: LVDS clock differential negative output |
| DPHYA_0P | I/O | H1 | MIPI: PORTA D-PHY Data[0] differential positive output<br>MIPI: PORTA C-PHY Data[0]-A output<br>LVDS: Video In/Out, Positive LVDS Data[0]<br>TTL: Video In/Out, TTL Data[0]<br>Alternate: Digital IO PAD as GPIO0 |
| DPHYA_0N | I/O | H2 | MIPI: PORTA D-PHY Data[0] differential negative output<br>MIPI: PORTA C-PHY Data[0]-B output<br>LVDS: Video In/Out, Negative LVDS Data[0]<br>TTL: Video In/Out, TTL Data[1]<br>Alternate: Digital IO PAD as GPIO1 |

| | | | |
|---|---|---|---|
| DPHYA_1P | I/O | J1 | MIPI: PORTA D-PHY Data[1] differential positive output<br>MIPI: PORTA C-PHY Data[0]-C output<br>LVDS: Video In/Out, Positive LVDS Data[1]<br>TTL: Video In/Out, TTL Data[2]<br>Alternate: Digital IO PAD as GPIO2 |
| DPHYA_1N | I/O | J2 | MIPI: PORTA D-PHY Data[1] differential negative output<br>MIPI: PORTA C-PHY Data[1]-A output<br>LVDS: Video In/Out, Negative LVDS Data[1]<br>TTL: Video In/Out, TTL Data[3]<br>Alternate: Digital IO PAD as GPIO3 |
| DPHYA_2P | I/O | K1 | MIPI: PORTA D-PHY clock differential positive output<br>MIPI: PORTA C-PHY Data[1]-B output<br>LVDS: Video In/Out, Positive LVDS Data[2]<br>TTL: Video In/Out, TTL Data[4]<br>Alternate: Digital IO PAD as GPIO4 |
| DPHYA_2N | I/O | K2 | MIPI: PORTA D-PHY clock differential negative output<br>MIPI: PORTA C-PHY Data[1]-C output<br>LVDS: Video In/Out, Negative LVDS Data[2]<br>TTL: Video In/Out, TTL Data[5]<br>Alternate: Digital IO PAD as GPIO5 |
| DPHYA_3P | I/O | L1 | MIPI: PORTA D-PHY Data[2] differential positive output<br>MIPI: PORTA C-PHY Data[2]-A output<br>LVDS: Video In/Out, Positive LVDS Data[3]<br>TTL: Video In/Out, TTL Data[6]<br>Alternate: Digital IO PAD as GPIO6 |
| DPHYA_3N | I/O | L2 | MIPI: PORTA D-PHY Data[2] differential negative output<br>MIPI: PORTA C-PHY Data[2]-B output<br>LVDS: Video In/Out, Negative LVDS Data[3]<br>TTL: Video In/Out, TTL Data[7]<br>Alternate: Digital IO PAD as GPIO7 |
| DPHYA_4P | I/O | M1 | MIPI: PORTA D-PHY Data[3] differential positive output<br>MIPI: PORTA C-PHY Data[2]-C output<br>LVDS: Video In/Out, Positive LVDS Data[4]<br>TTL: Video In/Out, TTL Data[8]<br>Alternate: Digital IO PAD as GPIO10 |
| DPHYA_4N | I/O | M2 | MIPI: PORTA D-PHY Data[3] differential negative output<br>LVDS: Video In/Out, Negative LVDS Data[4]<br>TTL: Video In/Out, TTL Data[9]<br>Alternate: Digital IO PAD as GPIO11 |
| DPHYA_5P | I/O | N1 | LVDS: Video In/Out, Positive LVDS Data[5]<br>TTL: Video In/Out, TTL Data[10]<br>Alternate: Digital IO PAD as GPIO12 |
| DPHYA_5N | I/O | N2 | LVDS: Video In/Out, Negative LVDS Data[5]<br>TTL: Video In/Out, TTL Data[11]<br>Alternate: Digital IO PAD as GPIO13 |
| DPHYB_0P | I/O | T5 | MIPI: PORTB D-PHY Data[0] differential positive output<br>MIPI: PORTB C-PHY Data[0]-A output<br>LVDS: Video In/Out, Positive LVDS Data[6]<br>TTL: Video In/Out, TTL Data[12] |
| DPHYB_0N | I/O | R5 | MIPI: PORTB D-PHY Data[0] differential negative output<br>MIPI: PORTB C-PHY Data[0]-B output<br>LVDS: Video In/Out, Negative LVDS Data[6]<br>TTL: Video In/Out, TTL Data[13] |

| | | | |
|---|---|---|---|
| DPHYB_1P | I/O | T6 | MIPI: PORTB D-PHY Data[1] differential positive output<br>MIPI: PORTB C-PHY Data[0]-C output<br>LVDS: Video In/Out, Positive LVDS Data[7]<br>TTL: Video In/Out, TTL Data[14]<br>Alternate: Digital IO PAD as GPIO0 |
| DPHYB_1N | I/O | R6 | MIPI: PORTB D-PHY Data[1] differential negative output<br>MIPI: PORTB C-PHY Data[1]-A output<br>LVDS: Video In/Out, Negative LVDS Data[7]<br>TTL: Video In/Out, TTL Data[15]<br>Alternate: Digital IO PAD as GPIO1 |
| DPHYB_2P | I/O | T7 | MIPI: PORTB D-PHY clock differential positive output<br>MIPI: PORTB C-PHY Data[1]-B output<br>LVDS: Video In/Out, Positive LVDS Data[8]<br>TTL: Video In/Out, TTL Data[16]<br>Alternate: Digital IO PAD as GPIO2 |
| DPHYB_2N | I/O | R7 | MIPI: PORTB D-PHY clock differential negative output<br>MIPI: PORTB C-PHY Data[1]-C output<br>LVDS: Video In/Out, Negative LVDS Data[8]<br>TTL: Video In/Out, TTL Data[17]<br>Alternate: Digital IO PAD as GPIO3 |
| DPHYB_3P | I/O | T8 | MIPI: PORTB D-PHY Data[2] differential positive output<br>MIPI: PORTB C-PHY Data[2]-A output<br>LVDS: Video In/Out, Positive LVDS Data[9]<br>TTL: Video In/Out, TTL Data[18]<br>Alternate: Digital IO PAD as GPIO4 |
| DPHYB_3N | I/O | R8 | MIPI: PORTB D-PHY Data[2] differential negative output<br>MIPI: PORTB C-PHY Data[2]-B output<br>LVDS: Video In/Out, Negative LVDS Data[9]<br>TTL: Video In/Out, TTL Data[19]<br>Alternate: Digital IO PAD as GPIO5 |
| DPHYB_4P | I/O | T9 | MIPI: PORTB D-PHY Data[3] differential positive output<br>MIPI: PORTB C-PHY Data[2]-C output<br>LVDS: Video In/Out, Positive LVDS Data[10]<br>TTL: Video In/Out, TTL Data[20]<br>Alternate: Digital IO PAD as GPIO6 |
| DPHYB_4N | I/O | R9 | MIPI: PORTB D-PHY Data[3] differential negative output<br>LVDS: Video In/Out, Negative LVDS Data[10]<br>TTL: Video In/Out, TTL Data[21]<br>Alternate: Digital IO PAD as GPIO7 |
| DPHYB_5P | I/O | T10 | LVDS: Video In/Out, Positive LVDS Data[11]<br>TTL: Video In/Out, TTL Data[22]<br>Alternate: Digital IO PAD as GPIO10 |
| DPHYB_5N | I/O | R10 | LVDS: Video In/Out, Negative LVDS Data[11]<br>TTL: Video In/Out, TTL Data[23]<br>Alternate: Digital IO PAD as GPIO11 |
| DPHY_VSP | I/O | P1 | LVDS: Video In/Out, Positive LVDS VSYNC<br>TTL: Video In/Out, TTL VSYNC |
| DPHY_VSN | I/O | P2 | LVDS: Video In/Out, Negative LVDS VSYNC<br>TTL: Video In/Out, TTL Data[12] |
| DPHY_HSP | I/O | R1 | LVDS: Video In/Out, Positive LVDS HSYNC<br>TTL: Video In/Out, TTL HSYNC |
| DPHY_HSN | I/O | R2 | LVDS: Video In/Out, Negative LVDS HYSNC<br>TTL: Video In/Out, TTL Data[13] |
| DPHY_DEP | I/O | R4 | LVDS: Video In/Out, Positive LVDS DE<br>TTL: Video In/Out, TTL Data[DE] |

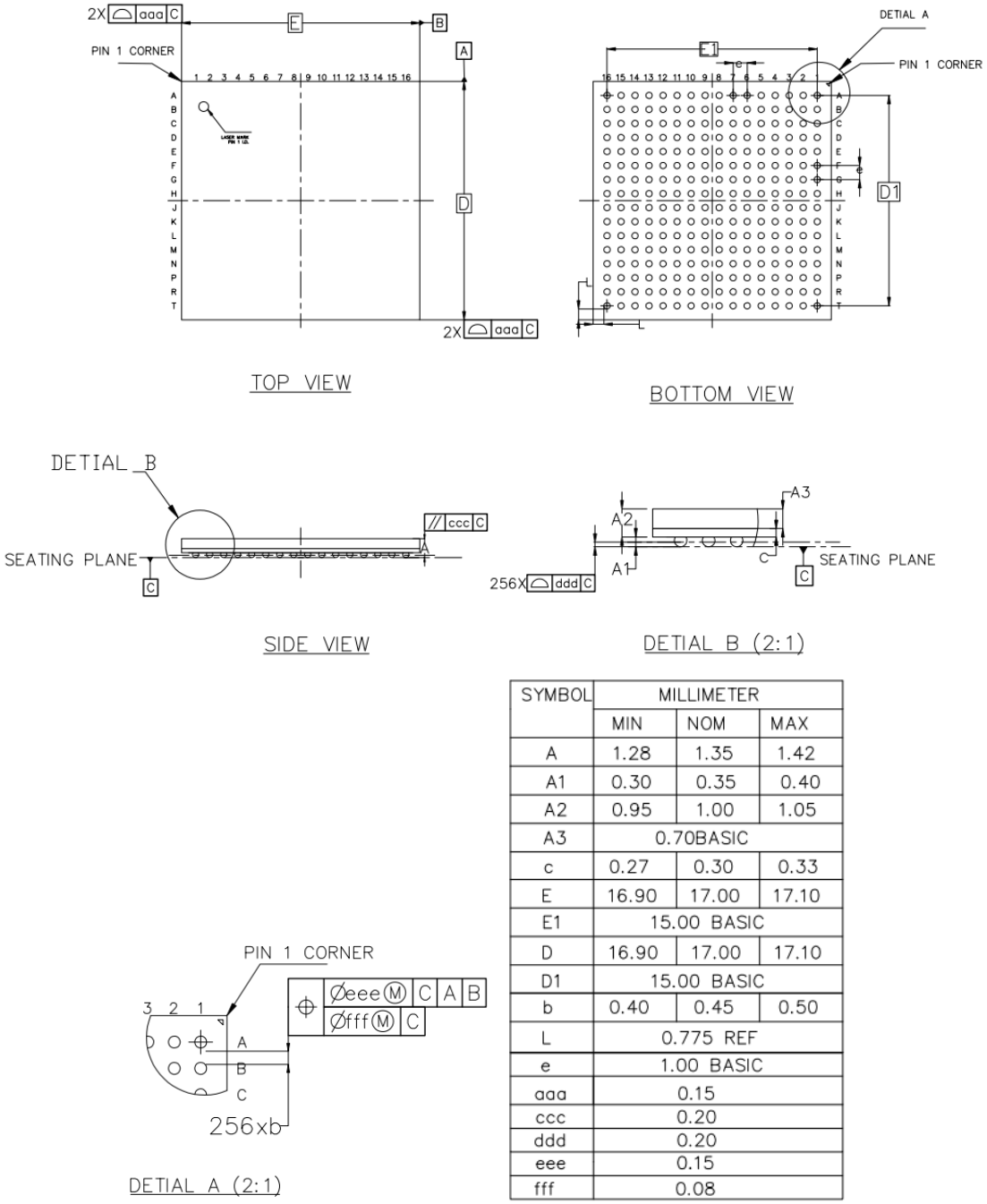
| | | | |
|---|---|---|---|
| DPHY_DEN | I/O | T4 | LVDS: Video In/Out, Negative LVDS DE<br>TTL: Video In/Out, TTL Data[24] |
| Digital pins | | | |
| I2C_SDA | I/O | L13 | Digital IO for I2C Data |
| I2C_SCL | I/O | L14 | Digital IO for I2C Clock |
| AUD1_SCLK | I/O | H14 | Digital IO PAD<br>Default: SCLK of Audio Bus 1<br>Alternate 1: GPIO3 for internal MCU control<br>Alternate 2: ADC_D2 |
| AUD1_MCLK | I/O | H13 | Digital IO PAD<br>Default: MCLK of Audio Bus 1<br>Alternate 1: GPIO2 for internal MCU control<br>Alternate 2: ADC_D3 |
| AUD1_D0 | I/O | J16 | Digital IO PAD<br>Default: Data0 of Audio Bus 1<br>Alternate 1: GPIO0 for internal MCU control<br>Alternate 2: UART0 TX for internal MCU control<br>Alternate 3: ADC_D0 |
| AUD1_D1 | I/O | J15 | Digital IO PAD<br>Default: Data1of Audio Bus 1<br>Alternate 1: GPIO10 for internal MCU control<br>Alternate 2: PWM0 output |
| AUD1_D2 | I/O | J14 | Digital IO PAD<br>Default: Data2 of Audio Bus 1<br>Alternate 1: GPIO11 for internal MCU control<br>Alternate 2: PWM1 output |
| AUD1_D3 | I/O | J13 | Digital IO PAD<br>Default: Data3 of Audio Bus 1<br>Alternate 1: GPIO12 for internal MCU control<br>Alternate 2: PWM2 output |
| AUD1_D4 | I/O | H16 | Digital IO PAD<br>Default: Data4 of Audio Bus 1<br>Alternate 1: GPIO13 for internal MCU control<br>Alternate 2: PWM3 output |
| AUD1_D5 | I/O | H15 | Digital IO PAD<br>Default: Data5 of Audio Bus 1<br>Alternate 1: GPIO1 for internal MCU control<br>Alternate 2: UART0 RX for internal MCU control<br>Alternate 3: ADC_D1 |
| AUD2_SCLK | I/O | F14 | Digital IO PAD<br>Default: SCLK of Audio Bus 2<br>Alternate 1: GPIO5 for internal MCU control<br>Alternate 2: ADV_TIM2 for internal MCU control |
| AUD2_MCLK | I/O | F13 | Digital IO PAD<br>Default: MCLK of Audio Bus 2<br>Alternate 1: GPIO4 for internal MCU control<br>Alternate 2: ADV_TIM1 for internal MCU control |
| AUD2_D0 | I/O | G16 | Digital IO PAD<br>Default: Data0 of Audio Bus 2<br>Alternate 1: GPIO7 for internal MCU control |
| AUD2_D1 | I/O | G15 | Digital IO PAD<br>Default: Data1of Audio Bus 2<br>Alternate 1: GPIO10 for internal MCU control |

| | | | |
|---|---|---|---|
| AUD2_D2 | I/O | G14 | Digital IO PAD<br>Default: Data2 of Audio Bus 2<br>Alternate 1: GPIO11 for internal MCU control |
| AUD2_D3 | I/O | G13 | Digital IO PAD<br>Default: Data3 of Audio Bus 2<br>Alternate 1: GPIO12 for internal MCU control<br>Alternate 2: Advanced Timer1 for internal MCU control |
| AUD2_D4 | I/O | F16 | Digital IO PAD<br>Default: Data4 of Audio Bus 2<br>Alternate 1: GPIO13 for internal MCU control<br>Alternate 2: Advanced Timer2 for internal MCU control |
| AUD2_D5 | I/O | F15 | Digital IO PAD<br>Default: Data5 of Audio Bus 2<br>Alternate 1: GPIO6 for internal MCU control<br>Alternate 2: CEC |
| GPIO4 | I/O | K16 | Digital IO PAD<br>Default: GPIO4<br>Alternate : Timer channel1 output |
| GPIO5 | I/O | K15 | Digital IO PAD<br>Default: GPIO5<br>Alternate : Timer channel2 output |
| GPIO6 | I/O | K14 | Digital IO PAD<br>Default: GPIO6<br>Alternate : UART0 RX for internal MCU control |
| GPIO7 | I/O | K13 | Digital IO PAD<br>Default: GPIO7<br>Alternate : UART0 TX for internal MCU control |
| GPIO8 | I/O | L16 | Digital IO PAD GPIO8 |
| GPIO9 | I/O | L15 | Digital IO PAD GPIO9 |
| QS_SCK | I/O | P15 | Quad-SPI Flash SCK |
| QS_CSB | I/O | P16 | Quad-SPI Flash CSB |
| QS_MOSI | I/O | N15 | Quad-SPI Flash MOSI |
| QS_MISO | I/O | N16 | Quad-SPI Flash MISO |
| QS_WPB | I/O | R15 | Quad-SPI Flash WPB |
| QS_HOLDB | I/O | R16 | Quad-SPI Flash HOLDB |
| INT | I | M15 | External Interrupt input |
| AVMUTE | I | M16 | AVMUTE input |
| JTAG1 | I/O | P9 | Default: TMS, Internal MCU programming pin<br>Alternate: General Interrupt Output Pin |
| JTAG2 | I | N9 | Default: TCK, Internal MCU programming pin<br>Alternate: AVMUTE Interrupt Output Pin |
| Misc pins | | | |
| RESETB | I | P10 | Reset Pin. Low for reset state, High for functional state. |
| XTALI | I | D4 | 25M Crystal Input |
| XTALO | O | D3 | 25M Crystal output |
| VMON | I/O | N4 | VBus0 Monitor Pin |
| CC0A | I/O | P4 | Type-C CC0 Pin1 |
| CC0B | I/O | N5 | Type-C CC0 Pin2 |
| USB_DP | I/O | N6 | USB 2.0 D+ Pin |
| USB_DM | I/O | P6 | USB 2.0 D- Pin |
| ALSB | I | C14 | Voltage signal input, determines 2 LSB of I2C slave address<br>GND: 00<br>VDD33/3: 01<br>2*VDD33/3: 10<br>VDD33: 11 |

| | | | |
|---|---|---|---|
| DDR_ZQ | I | M14 | Calibration, 240 ohm |
| DDR_VREFCA | I | M13 | |
| DDR_VREFDQ | I | N13 | |
| REXT400 | I | C16 | |

# 3 Electrical Specifications

# 4 Package Information




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.28 | 1.35 | 1.42 |
| A1 | 0.30 | 0.35 | 0.40 |
| A2 | 0.95 | 1.00 | 1.05 |
| A3 | 0.70BASIC | | |
| c | 0.27 | 0.30 | 0.33 |
| E | 16.90 | 17.00 | 17.10 |
| E1 | 15.00 BASIC | | |
| D | 16.90 | 17.00 | 17.10 |
| D1 | 15.00 BASIC | | |
| b | 0.40 | 0.45 | 0.50 |
| L | 0.775 REF | | |
| e | 1.00 BASIC | | |
| aaa | 0.15 | | |
| ccc | 0.20 | | |
| ddd | 0.20 | | |
| eee | 0.15 | | |
| fff | 0.08 | | |

Figure 18 Package Dimensions

# 5 Ordering Guide

# 6 Revision History

| Revision No. | Description | Date |
|---|---|---|
| V0.1 | Draft Initial Version for internal review. | Oct 30, 2024 |
| V0.2 | Update figures for clearer key features; Correct features description; Supplement package information | Nov 12, 2024 |
| V0.9 | Update pin diagram and description for BGA package; Update general information; add eDP description. | Jan 17, 2026 |

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