GSE1001

USB3.0 to 10/100/1000M Gigabit Ethernet Controller

April, 2026

Preliminary Product Specification

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1. General Description

1.1 General Information

The GSE1001 is a high-performance, low-power USB 3.0 to Gigabit Ethernet controller that supports both USB 3.0 SuperSpeed (5Gbps) and USB 2.0 (480Mbps) interfaces, while complying with the IEEE 802.3 10/100/1000M Ethernet standard. Equipped with a built-in hardware acceleration engine, which efficiently handles USB CDC class (such as NCM/ECM) . The GSE1001 delivers plug-and-play Gigabit Ethernet connectivity through standard USB ports, supporting a wide range of devices including consumer electronics (Desktops, Notebook PCs, Ultra-books) and specialized systems (docking stations, game consoles, digital home appliances, embedded systems).

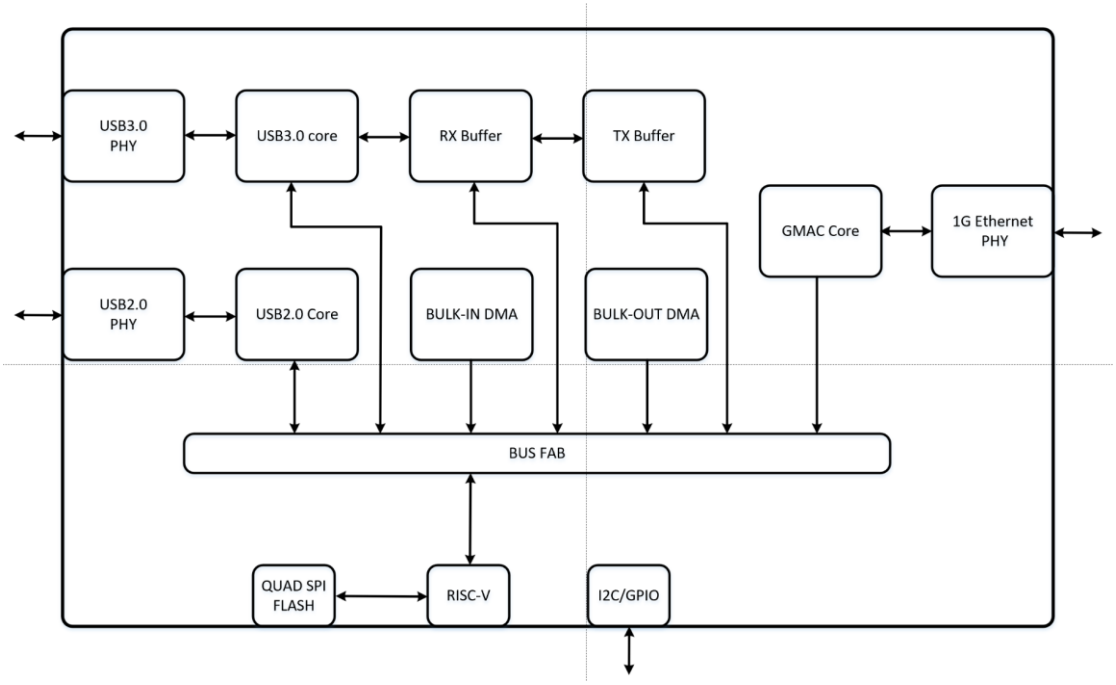


Figure 1. Top Diagram

1.2 Features

1.2.1 USB Features

- Compliant with USB 3.0/2.0 standards
- Bus-powered operation (no external power required)
- Supports USB suspend/resume modes (low-power design)
- Supports U1/U2/U3 low-power mode (USB 3.0)

1.2.2 Ethernet Features

- 10/100/1000M auto-negotiation with full-duplex mode
- IEEE 802.3az Energy-Efficient Ethernet (EEE) compliance
- Integrated Gigabit Ethernet PHY layer
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Built-in switching regulator and LDO regulator
- Supports hardware CRC (Cyclic-Redundancy Check) function

1.2.3 Performance Features

- Hardware-based TCP/IP checksum offload
- Jumbo frame support (up to 9KB packet size)
- Built-in DMA engine for high-efficiency data transfer

1.2.4 System Features

- Embedded internal MCU
- Embedded internal Flash
- External 25MHz Crystal required
- Available Pins for UART/ GPIO

1.3 Function Description

1.3.1 USB Interface

The SIE integrates a robust, hardwired USB protocol engine that relieves the firmware from managing USB interface operations. It takes full responsibility for generating handshake signals and responses for all endpoint types (Bulk-IN, Bulk-OUT, and Interrupt-IN). To complete its design, the integrated analog transceiver meets all driver and receiver requirements of the USB 3.0 Specification.

1.3.2 USB Configurations

GSE1001 supports multiple USB Ethernet classes, including ECM, NCM, and RNDIS. It is compatible with various operating systems such as Windows, Linux, and macOS, and operates without the need for additional drivers, ensuring plug-and-play functionality.

Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to completely describe the USB device. This pipe also provides the register read and write to the GSE1001.

Endpoint 1 Bulk-IN

The maximum Bulk-IN packet size is 1024 bytes. Each Ethernet packet is transferred to the HOST by this Endpoint. If the Ethernet packet is larger than 1024 bytes, the GSE1001 splits the Ethernet packet into multiples of 1024 bytes. The HOST treats USB packets that are less than 1024 bytes or are equal to zero as End of Ethernet packets.

Endpoint 2 Bulk-OUT

The HOST sends the USB packet to Ethernet. If the Ethernet packet is larger than 1024 bytes, the Host will send the Ethernet packet in multiples of 1024 bytes. A USB packet that is less than 1024 bytes or is equal to zero is treated as an End of Ethernet packet. The Ethernet packet (containing multiple USB packets) will be queued in the TX Buffer and transmitted when possible. If the Ethernet packet is transmitted without error, the TX Buffer space that was occupied by the transmitted Ethernet packet will be released. If the

TX Buffer is full, the GSE1001 will respond with a NRDY when the host tries to Bulk-OUT more USB packets.

Endpoint 3 Interrupt-IN

The Interrupt Endpoint (EP3) can be used to poll t TX/RX flow control enable, Connection Speed, Duplex mode, and link status of the GSE1001.

1.3.3 PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the GSE1001 operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), or CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The GSE1001 PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

1.3.4 PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

1.3.5 High-Performance DMA

GSE1001 integrates a high-performance DMA controller that efficiently manages data transfers between the USB and Ethernet interfaces. By offloading this task to dedicated hardware, the DMA ensures that the Ethernet port can achieve its full 1000M bandwidth capacity. At the same time, it maximizes the performance potential of the USB interface, allowing the system to maintain high data throughput without burdening the main processor.

1.3.6 FW Update Function

With the GSE1001, firmware updates are effortless owing to its USB interface support. This "update-over-USB" capability allows for seamless in-system programming, enabling end-

users or technicians to easily deploy the latest features and performance optimizations. It significantly simplifies after-sales service and ensures your product stays up-to-date with minimal downtime.

2. Pin Description

2.1 Pin Diagram

QFN40 Pin definition is defined as below.

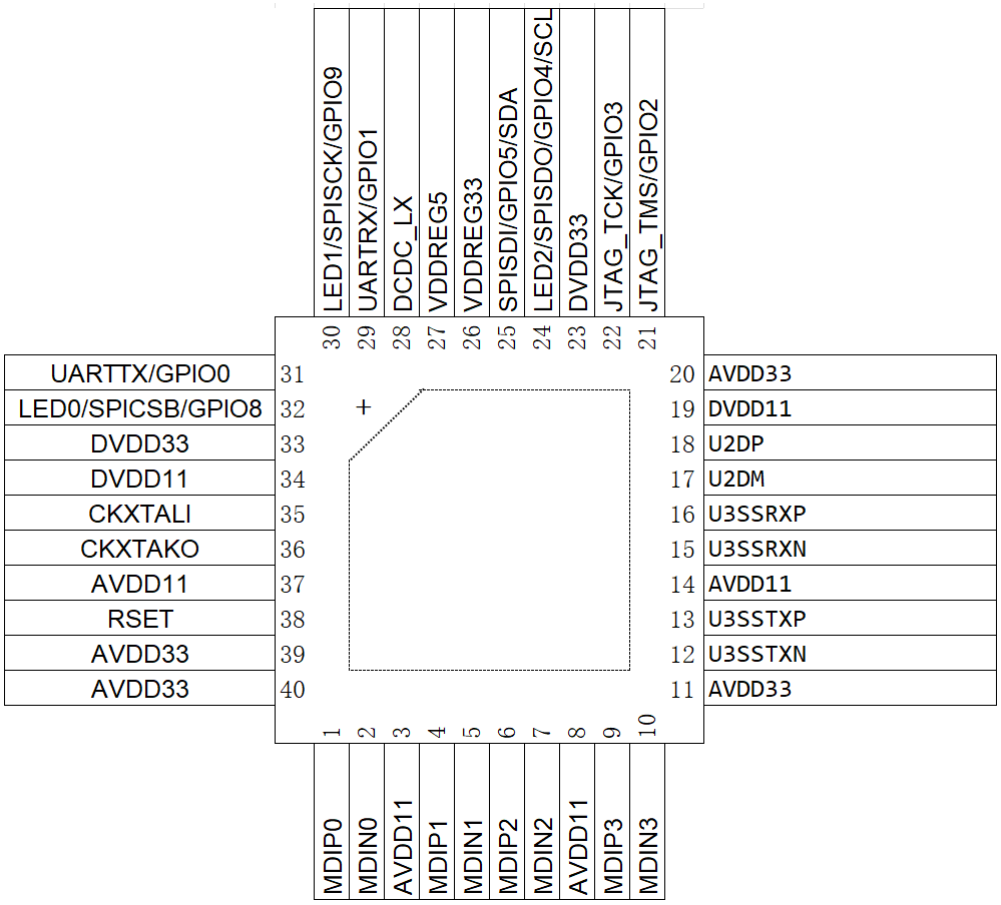


Figure 2. GSE1001 QFN40 Pin Diagram

Table 1. Clock Pins

Pin Name	Direction	Pin No.	Description
CKXTALI	I	35	Input of 25MHz Clock Reference
CKXTALO	O	36	Output of 25MHz Clock Reference

Table 2. Power and Ground Pins

Pin Name	Direction	Pin No.	Description
VDDREG33	I	26	Digital 3.3V Power Supply
VDDREG5	I	27	No Connect (NC)
AVDD33	I	11,20,39,40	Analog 3.3V Power Supply
DVDD33	I	23,33	Digital 3.3V Power Supply
AVDD11	I	3,8,14,37	Analog 1.1V Power Supply
DVDD11	I	19,34	Digital 1.1V Power Supply

Table 3. Regulator and Reference Pins

Pin Name	Direction	Pin No.	Description
DCDC_LX	O	28	Switching Regulator 1.2V Output
RSET	I	38	Reference (External Resistor Reference)

Table 4. Debug Pins

Pin Name	Direction	Pin No.	Description
JTAG_TCK	I	22	Two-Wire JTAG Clock Pin
JTAG_TMS	IO	21	Two-Wire JTAG Data Pin
UART TX	O	31	UART Transmit Data Pin
UART RX	I	29	UART Receive Data pin

Table 5. SPI Flash Pins

Pin Name	Direction	Pin No.	Description
SPI_SCK	O	30	SPI Flash Serial Clock
SPI_CSB	O	21	SPI Flash Chip Select
SPI_SDI	O	25	Input From SPI Flash Serial Data Output Pin
SPI_SDO	I	24	Output to SPI FLASH Serial Data Input Pin

Table 6. USB Pins

Pin Name	Direction	Pin No.	Description
U3SSRXP	I	16	USB 3.0 Super-Speed Receive Differential Pair
U3SSRXN	I	15	USB 3.0 Super-Speed Receive Differential Pair
U3SSTXP	O	13	USB 3.0 Super-Speed Transmit Differential Pair
U3SSTXN	O	12	USB 3.0 Super-Speed Transmit Differential Pair
U2DP	IO	18	USB 2.0 Differential Signal Pair
U2DM	IO	17	USB 2.0 Differential Signal Pair

Table 7. Transceiver Interface Pins

Pin Name	Direction	Pin No.	Description
MDIP0	IO	1	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX
MDIN0	IO	2	
MDIP1	IO	4	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX
MDIN1	IO	5	
MDIP2	IO	6	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair
MDIN2	IO	7	
MDIP3	IO	9	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- p
MDIN3	IO	10	

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

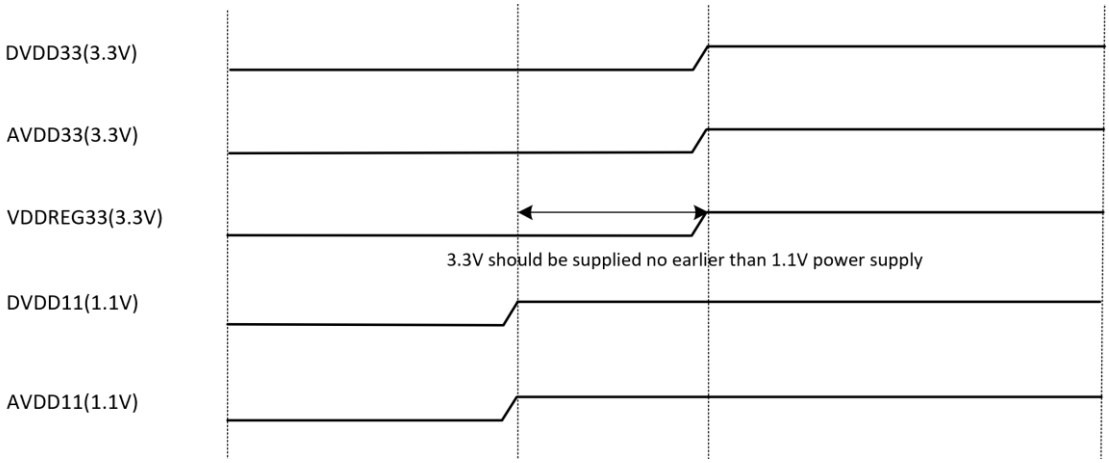


Figure 3. Power Up Sequence

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSE1001's operation temperature range is -20 ºC to 85 ºC. The maximum junction temperature is at 125 ºC. GSE1001 embeds internal temperature sensor for junction temperature read back.

3.2.2 Electrical Conditions

Table 8. Absolute Maximum Ratings

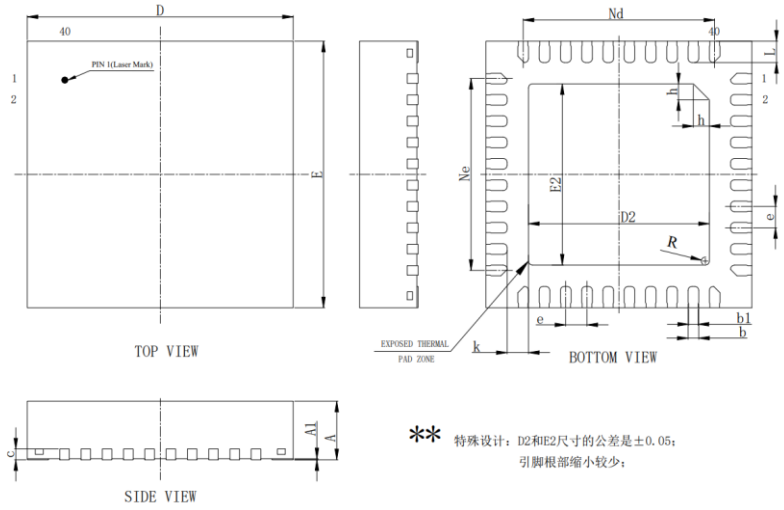
Power Domain	Minimum	Typical	Maximum
DVDD33	-0.5V	3.3V	5.0V
AVDD33	-0.5V	3.3V	5.0V
DVDD11	-0.3V	1.1V	1.8V
AVDD11	-0.3V	1.1V	1.8V
VDDREG33	-0.5V	3.3V	5V
VDDREG5	NC		

Table 9. Functional Operation Conditions

Power Domain	Minimum	Typical	Maximum
DVDD33	3.0V	3.3V	3.6V
DVDD11	1.06V	1.1V	1.32V
AVDD33	3V	3.3V	3.6V
AVDD11	1.06V	1.1V	1.32V
VDDREG33	3.0V	3.3V	3.6V
VDDREG5	NC		

Note: Recommend to use 1.2V In DVDD11/AVDD11 Power Domain.

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.10	1.15
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.18REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	3.35	3.40	3.45
e	0.40BSC		
Nd	3.60BSC		
Ne	3.60BSC		
E	4.90	5.00	5.10
E2	3.35	3.40	3.45
L	0.35	0.40	0.45
h	0.25	0.30	0.35
R	0.075REF		
k	0.35	0.40	0.45

Figure 4. Package Dimensions (QFN40)

5. Ordering Guide

Table 10. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSE1001	–20°C to +85°C	QFN40	Tray

6. Revision History

Table 11. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Nov 5, 2025
V0.2	Refresh PIN and Function Description	April 10, 2026

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